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Investigation of the Power Grid Accuracy by CMOS Transistor Network using Matlab/ Simulink

A B S T R A C T

The design and analysis of the power distribution and supply system on a chip is a complex issue. The ideal network consists of millions of transistors, which act as energy consumers. This large number makes them complex in terms of design and analysis. Building typical algorithms with logical gates and working automatically is the best way to solve the problem of power grid complexity. In this research, it was proposed to design a new model for consumers on the basis of effective resistance. passive elements were used only in this model and based on the actual resistance and capacity of the logical gates. Consumers and power grids can adopt computational physics methods and consider each group of consumers in each subnet as within total circuits. Emphasis is placed on the interaction between consumers for energy distribution network and energy supply. Using Matlab/ Simulink, accuracy of the system is verified to determine the technical issues related to the operation of the system for power networks.

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التحقيق من دقة شبكات القدرة الكهربائية المستخدمة لترانزستورات CMOS باستخدام برنامج الماتلاب

الخلاصة

شبكات الطاقة معقدة لوجود فيها اعداد كبيرة من الترانسستورات تتجاوز الملايين حيث ان هذا العدد الكبير يؤدي الى جعلها معقدة من حيث التصميم وايضا التحليل. ان بناء خوارزميات نموذجية تحتوي على بوابات منطقية وتعمل اوتوماتيكيا هو الطريقة المثلى لحل مشكلة تعقيد شبكات الطاقة. في هذا البحث تم اقتراح تصميم نموذجا جديدا للمستهلكين على اساس وجود مقاومة فعالة حيث تم استخدام عناصر سلبية في هذا النموذج وبالاعتماد على حساب المقاومة والسعة الفعالتين للبوابات المنطقية حيث كل ساعة من الوقت يتم تبديد الطاقة المتبددة والمخزنة و ان مجموع الطاقة يتم نمذجتها بالاعتماد على التفاعل الحاصل بين المستهلكين وشبكات الكهرباء و يمكن اعتماد طرق فيزيائية حسابية واعتبار كل مجموعة من المستهلكين في كل شبكة فرعية هي ضمن الدوائر الكلية.تم التركيز على التفاعل ما بين شبكات التوزيع والمستهلكين لتلك الطاقة. وباستخدام الماتلاب / المحاكاة يتم التحقق من دقة عمل النظام وذلك لتحديد المواضيع التقنية ذات الصله بتشغيل النظام لشبكات القدرة.

1. INTRODUCTION

One of the most difficult problems facing design in VLSI design is the efficient power distribution network in integrated circuits. The need for effective algorithms that take models in power distribution networks simplifies the problems of distribution networks. The increase in energy and the current demand for it and with the technological development increases the requirements of energy in the integrated circuits where the models are placed in the electrical networks in the form of elements of resistors and resistors. because of the presence of resistance and induction in the network there will be a decrease in voltage which is between the voltage inside and the logical gates [1]. This decrease can be expressed as LdI/dtor IR-drop which is due to induction and resistance respectively.

The main challenges faced by chip designers are signal integrity, which has been demonstrated by recent developments in technical processes in the CMOS system, which works toward the 90 nm area. Increased energy consumption and higher operating frequencies in VLSI circuits make the design and analysis of power distribution networks critical. The increase of the resistance and the rate of the current density in the unit length of the wire depends on the size of the effective bonding of this grid. As well as technological scaling reduces the level of processing voltage and the noise of power supply is relatively low and the reason is that the ratio of peak noise to the actual energy value processed increases with the technological scaling.

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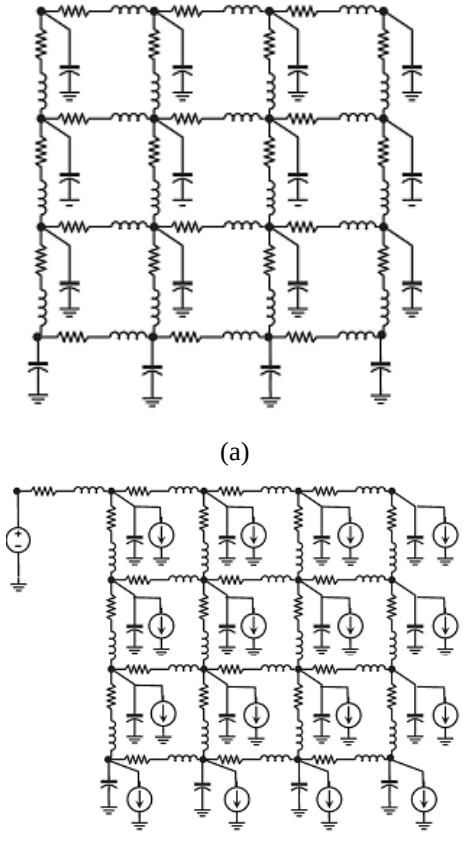
The noise of power processing is evident in the case of low voltage in the distribution networks and this negatively affects the operation of distribution networks that operate without interruption. Modeling of realistic on-chip power grid using the FDTD method by a group of authors at the University of Georgia modelled a multi layer on-chip distribution system using the Finite Difference Time Domain technique. The model consisted of 40 000 distributed current sources.

Power Grid Analysis in VLSI Designs [2], On-Chip Power Supply Noise and Reliability Analysis for Multi-Gigabit I/O Interfaces, Ralf Schmitt, Hai Lan, Ling Yang. Verified the power supply quality of the interface PHY is crucial to achieve multi-Gigabit data rates.

2. POWER DISITRUBTION NETWORKS

The simple RLC circuits are shown in Fig. 1 which can be used in this system and through the analysis and study of energy consumption and the number of devices and separation capacities. By solving the system,



(a)

(b)

Fig . 1. Basic schematic of a power grid (a) An RLC model of an on-chip power distribution network, and (b) A full RLC and conventional current consumer model as ideal current source.

2.1. Macro and Micro Circuits

The microcircuit model represents the use of energy in the circuits with the original gate. This feature can be expanded mainly to millions of small circuits that operate in parallel.

The current consumer and a cluster of the microcar-cuit in this model are represented as a microcircuit and a single simple, as shown in Fig. 1. The currents that flow through the network are causing the low voltage. There is a negative process between the feedback of the network currents and the noise and therefore the negative elements are used only to solve this problem.

The simulation of the system is performed in two separate steps. This is the first step in simulating all the devices. It is accurate and nonlinear, assuming that the voltage for each device is complete. Based on this, the current determined by the voltage is calculated. The devices are then designed separately and are considered as a separate source. Time The problem of distribution networks is solved by solving linear resistance networks. Ignoring nonlinear devices is wrong and special after a few repetitions [3]. The reason is that the ideal voltage is greater than the actual voltage of each device and during the nonlinear simulation step, which leads to the drawing of the currents of each instrument and its estimation and thus to the low voltage. The model is simplified and consists of resistors in the form of linear network and chip models to connect the power grid and the source of the current stream, all of which are also connected to the contract of the electricity network [4].

Simulating the power grid requires solving the differential equations that are formed through a typical approach like the modified nodal analysis [5]:

$$G\,x(t) + C\,\dot{x}(t) = u(t) \qquad (1)$$

where

G matrix of grid conductance.

C capacitive of the grid (decoupling capacitances) and inductive terms.

$x(t)$ time-varying vector of grid node voltages and currents through the inductors.

$u(t)$ vector of time-varying current sources attached to the grid nodes.

The standard cells that make these designs and through the rows of cells and the layout of the power trunks are able to distribute power between the cells as shown in Fig. 2.

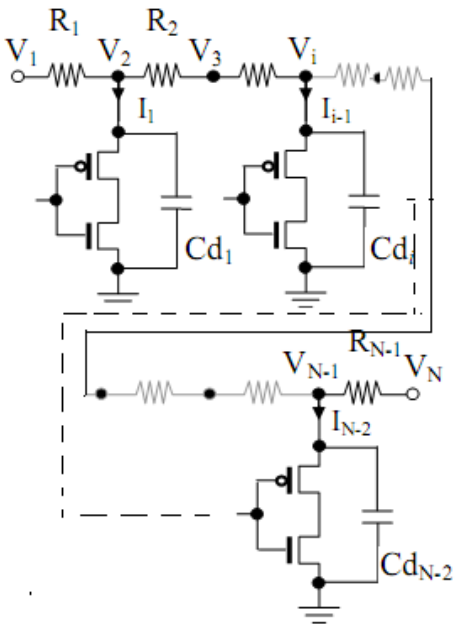


Fig. 2. Expanded view, local power supply with intermediate nodes and capacitances cellrow & semiglobal power grid of Going towards.

For the purpose of reducing the voltage level, the amount of interval required to achieve this requirement is calculated. This equation can be used:

$$P = Ct\, V2_{dd}\, f\, \gamma \quad (2)$$

where
P total consumption of chip power.
V_{dd} voltage of supply.
f clock frequency.
Ct capacitance of effective chip.
γ probability of transition.

2.2. Energy Dissipation

Changes in energy supply voltage (V_{dd}) strongly affect to the performance of cells connected to the local segment [6]. In order to find the sensitivity of the gate delay and to consider it as a function of changes in the power supply modifiers, we can use a simple model for a short channel of transistors in the saturation area. we can be written the (I_{ds}) as following:

$$I_{ds} = Vsat\, w\, (Vgs - Vt - Vds)C_{ox} \quad (3)$$

where
C_{ox} oxide capacitance.
Vgs source voltage of gate.
v_{sat} saturation velocity of carrier.
Vds source voltage.
Vt threshold voltage.

The sensitivity of gate delay, SD Vdd, to the power supply voltage changes can be expressed.

$$S^{D}_{V_{dd}} = \frac{V_{dd}.V_T - {v_T}^2 + E_C\, L\, V_{dd} + E_C\, L\, V_T}{(V_{dd} - V_T + E_C\, L)\,(V_{dd} - V_T)} \quad (4)$$

where
E_C critical electric field.
L channel length (ECL=1.4 V).
V_T assumed to be $V_{dd}/5$.

2.3. Effects of Interconnect Temperature, Barrier Thickness and Thin-Film

The surface scattering-governed resistivity ρ of a thin-film metal can be expressed in terms of ρ_0 as [7]:

$$\frac{\rho_0}{\rho_{thin\_film}} = 1 - \frac{3}{2k}(1 - p)\int_1^{\infty}\left(\frac{1}{x^3} - \frac{1}{x^5}\right)\frac{1 - e^{-kx}}{1 - pe^{-kx}}dx \quad (5)$$

where
$k = d/\lambda mfp$
d film smallest dimension.
p reflected electron fraction.

The parameter k effect on the surface dominance. when copper $p = 0.47$ and $\lambda mfp = 421$Å at 0 °C. and The amount of temperature affects the direction of the electrons

The larger coefficient temperature (α0) is different from the temperature coefficient of (α) layer resistance [6]. The relationship between interconnect resistance and temperature is a linear change and can be written as:

$$R = (\beta.\Delta T + 1)r0 \quad (6)$$

Table 1
Power tracks for Minimum number that needed to be routed on the power for different technology nodes for T = 105 °C and maximum of T.

NODE (µM)	J_0 (A/cm²) ×10⁵	Size of chip (mm²)	V_{dd} ,(V)	frequency (MHz)	P (W)	On- Chip C-Decap(nF)	T_{max} (°C)	P/G pads	Global pitch (nm)	Semi-global pitch (nm)	Global layer line	Semi-global line	R-local (kΩ/m)
0.17	5.7	440	1.6	1100	100	240	110	1520	1000	630	2.1	1.9	74.2
0.12	9.5	440	1.5	1800	140	300	130	2000	760	460	2.4	2.0	120.8
0.1	13	610	1.1	3100	160	330	140	2000	550	330	2.6	2.3	215.5
0.06	19	710	0.8	5200	170	370	170	2400	380	230	2.7	2.4	429.8

where
$r0$ unit length resistance at reference.
β temperature coefficient of resistance (1/°C).

Depending on the effects of thin scattering and surface barriers, it is possible to write the equation of interconnect resistance as following:

$$R = r_0\left(\frac{\rho}{\rho_0}\right)_{\text{thin\_barrier}_{\text{eff}}\left(1+\beta\frac{\alpha}{\alpha_0}\Delta T\right)} \quad (7)$$

The presence of such significant technological constraints with the effects of technological scaling on metal resistance leads to more realistic block resistance, which for each unit length of expected bulk resistance [8].

2.4. Rule Satisfaction of Power Network Electromigration

Using Table 1 the minimum-width gridlines require several technologies to satisfy EM rules for semi and global tiers as shown in Table 2. The increase in the density of the electricity network is more than expected through the transformation from global lines to semi-global and this is due to the decrease in the line as shown in Table 2.

Table 2
A local power distribution network for a typical standard cell.

NODE (μM)	T_{MAX} global (℃)	T_{MAX} Semiglobal (℃)	j_m / j_0	Global Tracks-100 ℃	Global tracks-T_{max}	Semiglobal - 100 ℃	Semiglobal tracks-T_{max}
0.17	115	113	0 .7	520	700	1550	2040
0.12	125	120	0 .6	590	1250	2440	3500
0.1	158	140	0 .4	1450	3900	4410	10010
0.06	165	150	0 .3	2330	7200	6930	18370

3. VOLTAGE DROP IN POWER NETWORK (GLOBAL/SEMI-GLOPAL

The system of Eq. (1) can be constructed by relying on the minimum number of power grid lines calculated from the Eq. (6) in each node and for each of the global and semi-global networks. Voltage values can be found in pin power on the basis of the worst value of low voltage. All of the above cases can be determined by studying the effect of decoupling capacitors

It is possible to use a number of the paths shown in Table 2 to separate the capacitors. Therefore, the voltage reduction ratio is severe. We need less than 10% voltage reduction in the ideal direction. Fig. 3 shows the worst low voltage.

The capacitors of the total separation can be calculated using the Eq. (2) and the Table 1. The condensates of the separation are supposed to be evenly distributed on the surface of the substrate.

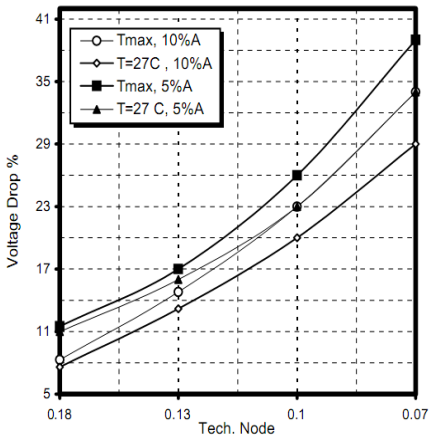


Fig. 3. Voltage drop percentage vs. technology node.

Fig. 4 shows the worst case of low voltage in global and semi-global networks, which use 10% of the routing area of the power grid and with the use of capacitor chip separation. The low voltage reaches an acceptable level of 0.17 µm technology and for holding the 130 nm technology where the voltage drop reaches 10%. The separation of the chip is 5% of the substrate

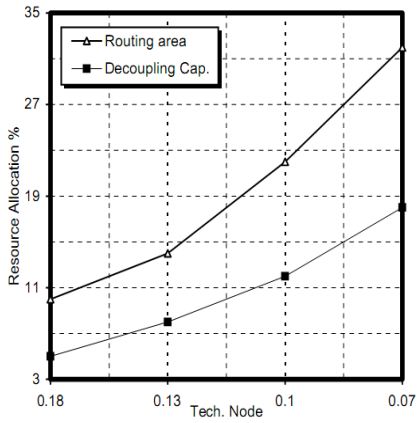


Fig. 4. percentage of the allocated resources to voltage drop for future technologies.

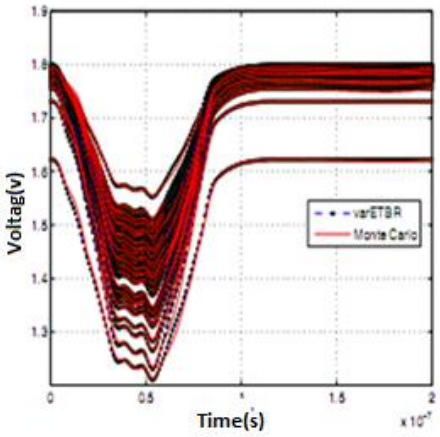


Fig. 5. Transient waveform at the 1000th node.

4. RESULTS AND DISSCUSSION

The most important negative phenomena that affect the performance of the guest of integrated circuits in the distribution of energy is the low voltage which makes the circuit work slowly and that the reduction of the acute voltage leads to confusion in the work of the circuits and cause logical errors. The decoupling capacitors between the nodes and ground grid is connected to the supply

networks and this leads to reduced fluctuations in the supply voltage. The decoupling capacitors are designed to store electrical charges. In the event of energy fluctuations, they are compensated from the stored charge and thereby prevent fluctuations in the power supply. That all kinds of low-voltage grid processing on the power chip are assumed to be connected to specific levels by margin of mass. When a significant reduction in the voltage occurs in the distribution network it leads a violation of the static logic and a failure in dynamic logic. for example, a 10% reduction in voltage in the network design and with the advantage of technology and 0.17 µm size increases the delay in switching devices and may reach 7%. This means that the main goal of the distribution design for networks is to obtain the lowest acceptable voltage fluctuation during the slides Which is about 10% of the normal distribution voltage and with the electrical reliability of the power distribution networks and to obtain such a network and working at: the minimum limits of the metal bonding area as shown in Figs. 3 and 4. The reason for the effective low voltage effect on the chip are:

(a) The sharp drop in voltage, which is caused by the largest drop in the chip in the interconnect line of the resistances.
(b) The induction of pin beams leads to a decrease in inductive voltage(*di*/*dt* nois).

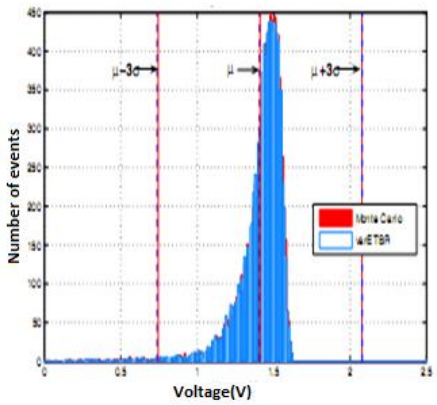


Fig. 6. Voltage distribution at the 1000th node.

The simultaneous conversion noise(SSN) or ground recoil causes rapid changes in the current through the parasitic inputs in the energy distribution networks and finding solutions for the *di*/*dt* and IR Separate detectors are added to the worst voltage mode so that the situation is pessimistic because of the angle of the situation The error is due to the contributing factors. This is a small occurrence as shown in Figs. 5 and 6. This is why we need an integrated packet and network chip level of power processing and accurate analysis models for voltage changes resulting from each factor.

5. CONCLUSIONS

The main issue in the analysis of power distribution network is the huge size of the problem. Simulating all the nonlinear devices in the chip together with the entire power grid is computationally infeasible. the larger size of the problem in power distribution networks is one of the main issues in the analysis of that network We have further highlighted the importance of low voltage effects and also focused on technology scaling and bonding in addition to temperature effects and the reliability of electro-magnetic Copper connections have been focused on and increased resistance due to the thickness of the limited barrier and dispersion of the electron surface and the consideration of low voltage analysis in power supply networks In all types of local fastening lines, the effects of scattering and thickness of the barrier should be taken into account, in addition to the fact that the temperature has an effective role in increasing the resistance of the metal at the global and sub-global levels One of the main reasons for the low performance in the energy distribution systems is the low electrical voltage in that system and that this factor has an effective role in the design policies of bonding and signal safety instructions. It is clear that there should be new guiding principles and principles for the allocation of materials for a metal zone and capacitors separated on a chip used for future technology for the purpose of reducing voltage change in power distribution networks. By studying the effect of non-uniform temperature and hot spots on the resistance of global joints, according to the data, capacitances of decoupling for the hot spots area must be adjusted.

REFERENSES

[1] Kogel T, et al. A modular simulation framework for architectural exploration of on-chip interconnection networks. *Proceedings of the 1st IEEE/ACM/IFIP international conference on Hardware/software codesign and system synthesis*: ACM; 2003. pp. 7-12.
[2] Hemani A, et al. Network on chip: An architecture for billion transistor era. *Proceeding of the IEEE NorChip Conference*. Jaipur, India; 2009. pp. 110-116.
[3] Chen HH, Ling DD. Power supply noise analysis methodology for deep-submicron VLSI chip design. *The 34th annual Design Automation Conference*: ACM; 1997. pp. 638-643.
[4] Chowdhury R, Bo Ruahm T. Design of a microgrid system. *International Journal of Innovative Research in Science, Engineering and Technology* 2015; **4** (7): 5262-5269.
[5] Manna K, Singh S, Chattopadhyay S, Sengupta I. Preemptive test scheduling for network-on-chip using particle swarm optimization. VLSI Design and Test: Springer; 2013. pp. 74-82.
[6] Chandrakasan AP, Bowhill WJ, Fox F. Design of high-performance microprocessor circuits. 3rd ed. ed. New York: Wiley-IEEE press; 2010.
[7] Gonzalez R, Gordon BM, Horowitz MA. Supply and threshold voltage scaling for low power CMOS. *IEEE Journal of Solid-State Circuits* 1997; **32** (8): 1210-1216.
[8] Lasseter RH. Micro-grids: IEEE power engineering society winter meeting, New York, NY, 2015; **8** (01): 305-308.
[9] Consoli E, Giustolisi G, Palumbo G. An accurate ultra-compact I–V model for nanometer MOS transistors with applications on digital circuits. *IEEE Transactions on Circuits and Systems I* 2012; **59** (1): 159-169.
[10] Gharpurey R, Kinget P. Ultra wideband: circuits, transceivers and systems. Ultra Wideband: Springer; 2008. pp. 1-23.