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Design and Implementation of Decimation Filter for 13-bit Sigma-Delta ADC Based on FPGA

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Abstract

A 13 bit Sigma-Delta ADC for a signal band of 40K Hz is designed in MATLAB Simulink and then implemented using Xilinx system generator tool. The first order Sigma-Delta modulator is designed to work at a signal band of 40 KHz at an oversampling ratio (OSR) of 256 with a sampling frequency of 20.48 MHz. The proposed decimation filter design is consists of a second order Cascaded Integrator Comb filter (CIC) followed by two finite impulse response (FIR) filters. This architecture reduces the need for multiplication which is need very large area. This architecture implements a decimation ratio of 256 and allows a maximum resolution of 13 bits in the output of the filter. The decimation filter was designed and tested in Xilinx system generator tool which reduces the design cycle by directly generating efficient VHDL code. The results obtained show that the overall Sigma-Delta ADC is able to achieve an ENOB (Effective Number Of Bit) of 13.71 bits and SNR of 84.3 dB.

Keywords: Sigma-Delta modulation, Decimation filter, A/D conversion, Oversampling, FPGA, VHDL.

تصميم وتنفيذ مرشح القاتل للمحول التناظري الى رقمي نوع سيكما دلتا بدقة 13 bit باستخدام البوابات القابلة للبرمجة حقلياً

الخلاصة

تم تصميم وتنفيذ المحول التناظري الى الرقمي نوع سيكما دلتا بدقة 13 bits وبحزمة ترددية مقدارها 40 KHz باستخدام برنامج الماتلاب ومولد النظام. تم تصميم المضمن سيكما دلتا ذو الرتبة الاولى عند حزمة ترددية مقدارها 40 KHz، و (Oversampling ratio) مقدارها 256 ،وتردد نمذجة مقداره 20.48 MHz. يتكون مرشح (Decimation) المقترح من المرشح (CIC) ذو الرتبة الثانية ومرشحي الاستجابة محدد النبضة. المعمارية المقترحة لتنفيذ مرشح الـ(Decimation) تقلل من الحاجة إلى دائرة الضرب التي تحتاج مساحة كبيرة جداً عند التنفيذ. تعمل المعمارية المقترحة للمرشح الـ(Decimation) على تقليل تردد النمذجة بمقدار (512) وجعل الدقة في اخراج المرشح تساوي 13 bits. المعمارية المقترحة لتنفيذ مرشح الـ(Decimation) تقلل من الحاجة إلى دائرة الضرب التي تحتاج مساحة كبيرة جدا عند التنفيذ. تم تصميم وفحص المرشح (Decimation) باستخدام مولد النظام مما ساعد على تقليل دورة التصميم عن طريق توليد مباشر للكيان المادي الخاص بتنفيذ المرشح (Decimation). أظهرت النتائج النهائية ان مقدار نسبة إشارة المعلومات إلى الإشارة الضوضائية للمحول المقترح كانت تساوي 84.3 dB ،وأن مقدار الـ(ENOB) كان يساوي 13.71 bits.

الكلمات الدالة: المضمن سيكما-دلتا، المحول التناظري نوع سيكما-دلتا، البوابات القابلة للبرمجة حقليا، مرشح القاتل

Introduction

In many modern electronic systems the key components are the analog to digital converters. They provide the translation of a measured analog signal to a digital representation. In the digital form the data can be easily and accurately processed to extract the information desired. The process of converting the analog signal to a digital signal some time limits the speed and resolution of the overall system. Therefore, it is necessary to develop analog to digital converters that achieve both high speed and resolution. In particular, many instrumentation, communication, and imaging systems can benefit from such converters [1,2].

There are different types of analog to digital conversion techniques available today, each having its own advantages and disadvantages. Analog-to-digital converters are categorized into two types namely Nyquist rate converters and oversampling converters depending on the sampling rate. Sigma-delta ADCs come in oversampling converters group[3,4].

Oversampling converters reduce the requirements of analog circuitry at expense of faster and more complex digital circuitry [5,6]. Sigma Delta analog-to-digital converters need relatively imprecise analog circuits and digital decimation filtering [5].The sigma-delta ADC works on the principle of sigma-delta modulation. The sigma-delta modulation is a process for encoding high-resolution signals into lower resolution signals using pulse-density modulation. It samples the input signal at a rate much higher than the Nyquist rate. A sigma-delta ADC consists of an analog block of modulator and a digital block of decimator. The modulator samples the input signal at an oversampling rate, generating a one bit output stream and decimator is a digital filter or down sampler where the actual digital signal processing is done [6].

Sigma-Delta A/D CONVERTER

Figure (1) shows the block diagram of a Sigma-Delta A/D converter. It consists of a sigma-delta modulator and a decimation filter. The modulator can be realized using analog technique to produce a single bit stream and a digital Decimation filter to achieve a multi bit digital output thus completing the process of analog to digital conversion [4,6].

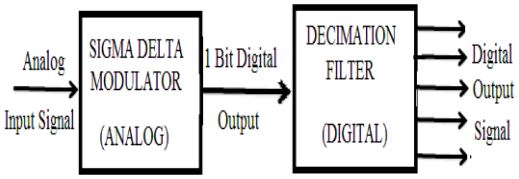

Fig. 1. Block diagram of Sigma-Delta A/D converter [4]

Sigma-Delta Modulator

The first order Sigma-Delta modulator consists of an analog difference node, an integrator, a 1- bit quantizer (A/D converter) and a 1-bit D/A converter in a feed- back structure. The modulator output has only 1-bit (two levels) of information, i.e., 1 or -1. Figure (2) shows first order Sigma-Delta modulator[7].

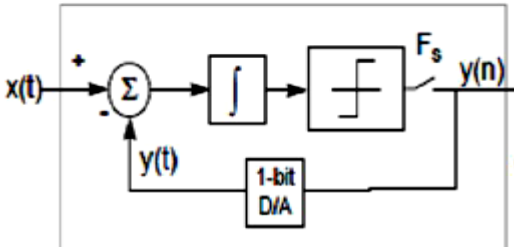

Fig. 2. First order Sigma-Delta modulator[7]

The relation between the input and output in the discrete time is shown as:

$$Y(z) = X(z) + (1- z^{-1}) \quad \ldots\ldots\ldots\ldots\ldots\ldots \quad (1)$$

The error introduced from the quantizer is pushed to the high frequency terms due to the term $(1-z^{-1})$ [8]. The key equations can be given by [9] :

$$\frac{Y(z)}{Q(z)} = 1- z^{-1} \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (2)$$

Where $z = e^{j2\pi f T_{ck}}$, then

$\frac{Y(z)}{Q(z)} = (1 - e^{-j2\pi f T_{ck}})$ .....(3)

Hence the noise shaping function is written as:

$S_y(f) = 2\, S_q(f)\, |1 - \cos(2\pi f T_{ck})|$ (4)

Where:

T_{ck}: is the clock frequency of Sigma-Delta modulator

fs = $\frac{1}{T_{ck}}$ (sampling frequency of Sigma-Delta modulator)

Where $S_q(f)$ is relatively flat for the low frequencies.

Figure (3) shows the spectrum of a first order Sigma-Delta noise shaping.

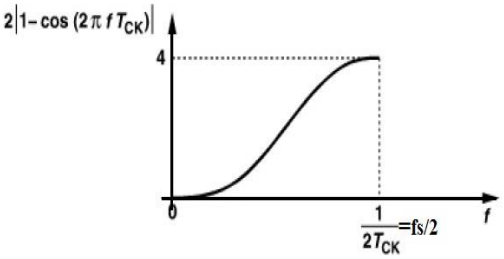

Fig. 3. Noise shaping of the 1st order modulator [9]

The sigma-delta modulator suffers from high quantization noise at high frequencies. To achieve high resolution, this quantization noise must be removed, and decimate or reduce the sample rate of the Sigma-Delta modulator output to the Nyquist rate which minimizes the amount of information for subsequent transmission, storage or digital signal processing [10].

Digital Filtering

The basic aim of the digital filter is to remove the quantization Noise at high frequencies due to using of sigma-delta modulator, reduce the sample rate of the Sigma-Delta modulator output to the Nyquist rate and increase the 1-bit or several-bit data word to high-resolution sample word. Practically it is impossible to implement a single filter that would meet the characteristic of decimation filter, because the order of such filters would be very high [11]. So it is necessary to divide the architecture of decimation filter into two parts: Cascaded integrator-comb (CIC) and FIR filters**.** The CIC filter is a combination of digital integrator and digital differentiator stages which execute the operation of digital low pass filtering and decimation. The CIC filter is a multiplier free filter that can accepts large rate changes. The CIC filter first performs the averaging process then follows it with the decimation. A simple block diagram of a first order CIC filter is shown in Figure (4)[12].

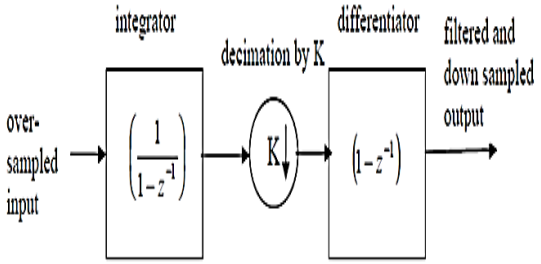

Fig. 4. Block diagram of CIC filter [12]

The integrator works at the sampling clock frequency, (f_s) while the differentiator works at down sampled clock frequency of (f_s/K). By operating the differentiator at lower frequencies, a saving in the power consumption is achieved. Equation (5) gives the magnitude response of a CIC filter at frequency (f) where (N) is the order of the filter[13].

$$|H(f)| = \left| \frac{Sin(\pi M f)}{Sin(\frac{\pi f}{K})} \right|^N \quad \text{.....(5)}$$

Figure (5) shows the frequency response of the CIC filter found using Equation (5). The aliasing bands $2f_c$ centered around multiples of the low sampling rate. As the number of stages in a CIC filter is increased, the frequency response has a smaller flat pass band. To overcome the magnitude droop, an FIR filter can be applied to achieve frequency response correction. Such filters are called “compensation filters" [13].

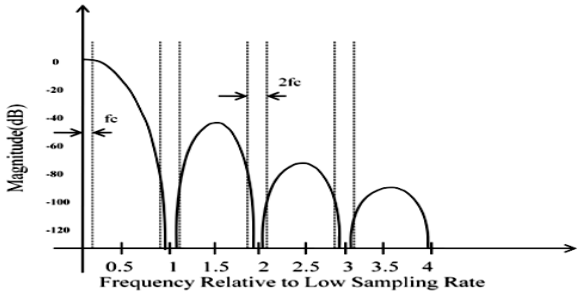

Fig. 5. Frequency response of a CIC filter [13]

Design and Simulation Methods

The proposed Sigma-Delta ADC used in this paper is shown in Figure (6) which consists of a sigma delta modulator followed by a Decimation Filter which is designed in MATLAB Simulink.

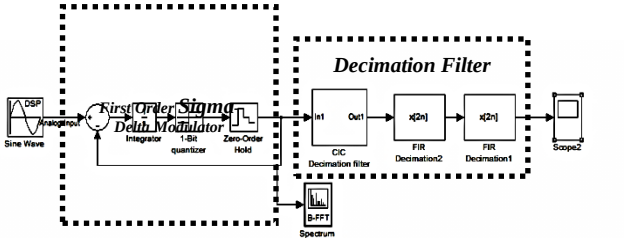

Fig. 6. MATLAB model of the Sigma-Delta ADC

The characteristics of the proposed Sigma-Delta ADC are shown in Table (1). A 13 bit Sigma-Delta ADC for a signal band of 40K Hz is designed in MATLAB Simulink and then the decimation filter has been designed using Xilinx system generator tool , which reduces the design cycle by directly generating efficient VHDL code .The VHDL code has been implemented on a Spartan 3E FPGA using ISE 14.1 tool.

The Simulink Model of first order Sigma Delta Modulator is shown in Figure (7). It consists of a difference operator, integrator, 1-bit quantizer, and a negative feedback.
The modulator achieves a SNR of 53.6 dB for a signal bandwidth of 40 KHz. The modulator operates with an oversampling ratio (OSR) of 256 and a sampling frequency of 20.48 MHz.

In order to remove the high quantization noise at high frequencies, the sample rate of the output of the Sigma-Delta modulator must be reduced to the Nyquist rate and to achieve high resolution the decimation filter should have the characteristics shown in Table 2.

Table 1. The characteristics of Sigma-Delta ADC

Parameters	Symbol	Value
Signal bandwidth:	BW	40 KHz
Sampling Frequency:	F_S	20,48 MHz
Over Sampling Ratio:	K	256
Modulator order:	M	1
Number of bits in modulator bit stream:	B_{Mod}	1
Number of bits in output of filter:	B	13

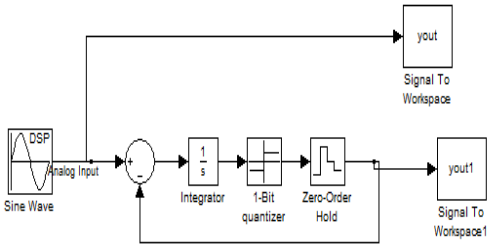

Fig. 7. MATLAB model of First Order Sigma-Delta Modulator

Table 2. Decimation filter characteristics

Filter parameters	Value
Sampling frequency:	F_s = 20.48 MHz
Down Sampling Ratio:	DSR = 256
Pass band frequency:	F_{pass} = 40 KHz
Stop band frequency:	F_{stop} = 41.6 KHz
Pass band Max ripple:	A_{pass} = 0.0005 dB
Stop band attenuation	A_{stop} = 90 dB

The decimation filter accepts the single bit stream from the modulator and converts it into a 13-bit digital output. Practically it is not possible to implement a single filter that would meet the characteristics of Table 2. The order

of such filter would be close to 5000. It is difficult to implement such a hardware filter. Therefore, it is needed to use a multi-stage approach, whereby the decimation is performed in several stages. The proposed decimation filter architecture is consists of three stages Second-order Cascaded Integrator Comb filter followed by two (FIR) filters, as shown in Figure (8).

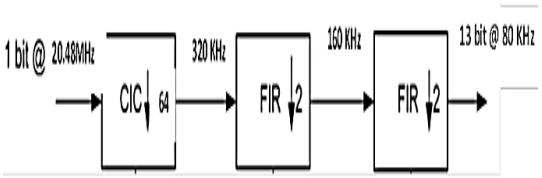

Fig. 8. Decimation filter architecture

The multistage architecture allows most of the filter hardware to operate at a lower clock frequency, and have lower hardware complexity when compared to a single state decimator. The frequency response of a Second order Cascaded Integrator Comb filter is shown in Figure (9).

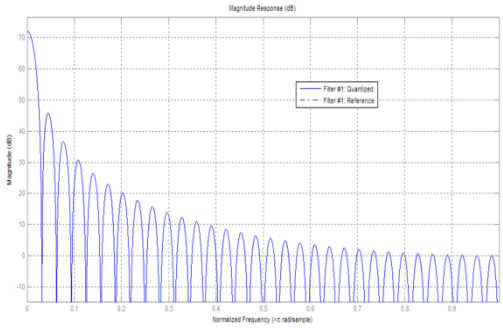

Fig. 9. Frequency response of a second order CIC filter

The input to the Cascaded Integrator Comb (CIC) filter is a 1-bit pulse density modulated signal from a first order sigma-delta modulator. Internal word width (W) for this design of CIC filter need to ensure that there is no run time overflow given by Equation (6) [4].

W = (1Sign bit) + (Number of input bits) + (Number of stages, N) log2 (Decimator factor) ……..(6)

In this paper, W = 1 + 1 + 2 log2(64) i.e. W=14

The output from the Cascaded Integrator Comb (CIC) filter is a (1 sign bit +13 resolution bits) digital output. To overcome the magnitude droop in Cascaded Integrator Comb (CIC) filter, two FIR filters has been used to achieve frequency response correction. The order of the designed FIR filters is 18 and 150 respectively. Figure (10) shows the frequency response of the designed FIR filters.

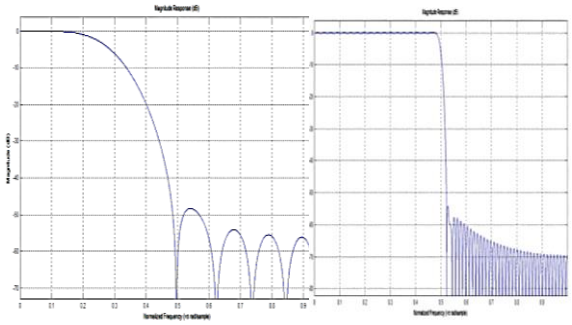

Fig.10. Frequency response of first and second FIR filter

For the first-order over sampled sigma-delta modulator and the second-order CIC filter used in the design, the desired output resolution is given by Equation (7)[7].

$$N_{final} = N_{i/p} + \frac{30\log K - 5.17}{6.02} \quad \text{.....(7)}$$

Where :
N_{final} is the final output resolution,
$N_{i/p}$ is the input resolution of the decimator.
So, for $K=256$, the output resolution achieved is 13 bits.

The proposed decimation filter has been designed using MATLAB Xilinx system generator tool, which reduces the design cycle by directly generating efficient VHDL code. Figure (11) shows the decimation filter designed in system generator. The VHDL code has been implemented on a Spartan FPGA using ISE 14.1 tool.

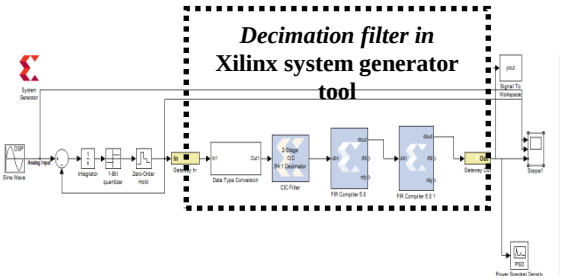

Fig. 11. Decimation filter designed in system generator

Results and Discussion

The output of first order Sigma-Delta modulator with a sampling frequency of 20.48 M Hz for a sine wave input of 1 Vpp and 20 KHz is shown in Figure (12).

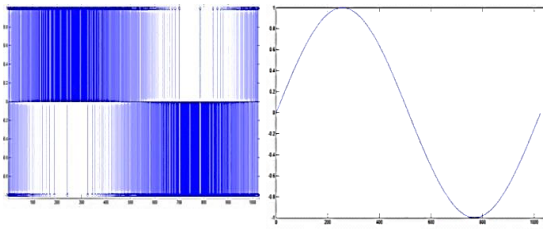

Fig.12. Transient response of first order Sigma-Delta modulator for a sine wave input of 20 KHz

It is clearly evident that the output (single bit) is a pulse width modulated in accordance with input sine wave. The number of 1's increases at the positive peak of the input sine wave and the number of -1's are more at the negative peak. There are equal number of 1's and -1's when the input signal is at zero amplitude, which is the expected response of a Sigma Delta Modulator.

Figure (13) shows the simulated power spectral density (PSD) of the proposed Delta Sigma modulator for a 20 KHz input sine wave.

As shown in Figure (13) the quantization noise shifted towards high frequency band. The modulator signal to noise ratio (SNR) was designed to be 53.5 dB for first-order output with an OSR of 256.

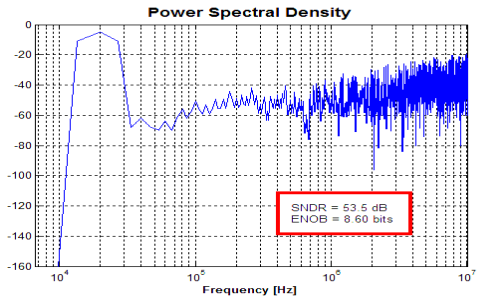

Fig.13. Power spectral density

Figure (14) shows the output spectrum of the decimation filter, it is clear that the decimation filter is able to remove the out-of-band noise effectively and increases the SNR. The complete ADC is able to achieve a resolution of 13.71 bits and SNR of 84.3 dB.

The output Power Spectral Density (PSD) of the decimation filter using Xilinx system generator tool was exactly the same as the result in MATLAB Simulink as shown in Figure (14). Figure (15) shows the digital output from decimation filter for 20 KHz analog signal

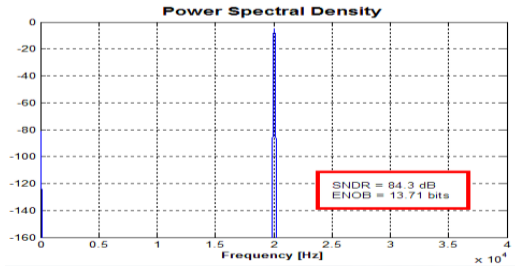

Fig. 14. Power spectral density (PSD) of output of decimation filter

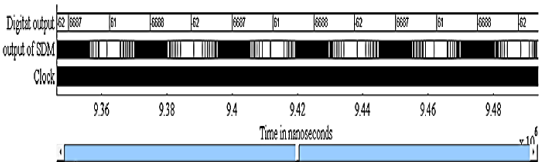

Fig.15. Digital output for analog signal 20 KHz

To implement the decimation filter in Spartan 3E the efficient VHDL code was directly generated from the design of the decimation filter in Xilinx system generator. Using Xilinx ISE to simulate the VHDL code which generated from system generator, the result of digital output from decimation filter for

20 KHz analog signal in Xilinx ISE simulation is shown in Figure (16).

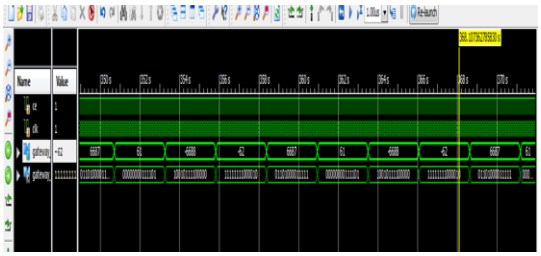

Fig. 16. Digital output for analog signal 20 KHz in Xilinx ISE

The result of Xilinx ISE simulation exactly the same as the result from MATLAB Simulink. Table (2) shows a summary of the resources utilized in the implementation of the decimation filter in Spartan 3E.

Table 2. Resource utilization for Spartan 3E

Device Utilization Summary			
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Flip Flops	723	9,312	7%
Number of 4 input LUTs	503	9,312	5%
Number of occupied Slices	496	4,656	10%
Number of Slices containing only related logic	496	496	100%
Number of Slices containing unrelated logic	0	496	0%
Total Number of 4 input LUTs	566	9,312	6%
Number used as logic	390		
Number used as a route-thru	63		
Number used as Shift registers	113		
Number of bonded IOBs	14	232	6%
Number of RAMB16s	3	20	15%
Number of BUFGMUXs	1	24	4%
Number of MULT18X18SIOs	3	20	15%
Average Fanout of Non-Clock Nets	2.22		

The decimation filter performance has been ascertained using the hardware co-simulation that uses Chipscope Pro Analyzer in ISE. The digital output result from implementing the decimation filter in Spartan 3E by using the chipscope for 20 KHz analog signal is shown in Figure (17).

By comparing digital signal obtained using chipscope with the digital signal obtained using MATLAB Simulink, it can be seen that the two digital signals are very similar and this mean that generation and implementation of the VHDL code in Spartan 3E is performed without any error.

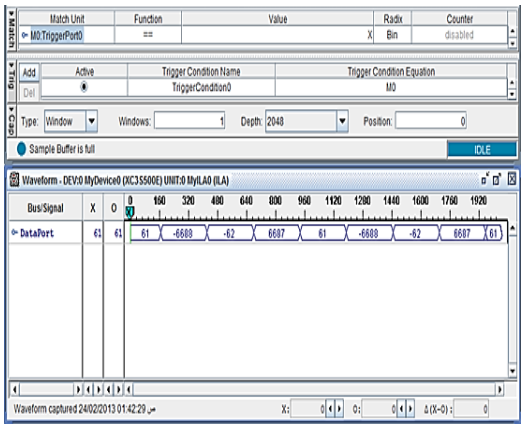

Fig. 17. Result of implementation the decimation filter in Spartan 3E

Because of similarity in time domain between two digital signals of simulation and implementation that shown in Figures (15) and (17), it can be assumed that the output spectrum of implementing the decimation filter is the same as the simulated output spectrum.

Conclusion

A complete sigma delta ADC is designed using a first order Sigma-Delta modulator and a Digital decimation filter with an OSR of 256. The multistage architecture reduces the need for multiplication which is need very large area to implement in hardware and allows most of the filter hardware to operate at a lower clock frequency which have lower hardware complexity when compared to a single state decimation filter. Digital decimation filter for Sigma Delta ADC is successfully implemented into Xilinx Spartan series FPGA. This ADC gives overall 13 bits resolution and SNR of 84.3 dB.

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