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Design of Current Mode MTCMOS Sense Amplifier with Low Power and High Speed

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Abstract

This paper involved the design and analysis of multi-threshold voltage CMOS (MTCMOS) current sense amplifier focusing on optimizing power and time delay. In this work the basic 6T SRAM structure was chosen and the simulation is implemented using ADS programs. The key to low power operation in the SRAM data path is to reduce the signal swings on the bit lines and the data lines. The power dissipation and delay of the sense amplifier circuit can be further reduced by using several low power and high speed techniques like MTCMOS. This technique can be used for solving the leakage power dissipation problem in the higher technology design. Simulated results show the current mode sense amplifier with MTCMOS technology has 0.82ns time delay and 0.395µW power dissipation. The designs and simulations in 0.25µm CMOS technology with supply voltage equal to 1.8 V have been carried out to evaluate the efficiency of the current mode sense amplifier with MTCMOS technique proposed.

Keywords: 6T SRAM cell, MTCMOS technology, Low power, High speed.

تصميم مكبر متحسس للتيار متعدد فولتيات العتبة (MTCMOS) ذات قدرة قليلة وسرعة عالية

الخلاصة

تناول هذا البحث تصميم وتحليل مكبر متحسس للتيار متعدد فولتيات العتبة (MTCMOS sense amplifier) والعمل على تقليل القدرة وزيادة سرعة التحسس.في هذا البحث تم اختيار 6T SRAM cell وتنفيذ المحاكاة باستخدام برنامج ADS. إن المفتاح الى قدرة عمل قليلة في مسار بيانات SRAMهي بتقليل مقدار تأرجح الإشارة على خطوط البت وخطوط البيانات.حيث إن استهلاك القدرة وزمن التأخير في دائرة المكبر المتحسس يمكن تقليلها الى ابعد حد باستخدام عدة تقنيات للقدرة القليلة والسرعة العالية مثل MTCMOS .هذه التقنية يمكن ان تستعمل لحل مشكلة القدرة المستهلكة في تصميم التقنيات المتقدمة.إن نتائج المحاكاة بينت بان المكبر المتحسس للتيار ذو فولتيات العتبة المتعدد يملك تأخيراً في الزمن قدرهُ 0.82ns وقدرة مستهلكة قدرها 0.395µW. هذا التصميم والمحاكاة نفذ في تقنية (CMOS-0.25µm) ومصدر مجهز قدرهُ 1.8V للمكبر المتحسس للتيار متعدد فولتيات العتبة المقترح.

الكلمات الدالة: خلية ذاكرة ثابتة 6T ، تقنيه تعدد فولتيات العتبة، قدره استهلاك قليلة، سرعة استجابة عالية.

Introduction

Sense Amplifier (SA) is the most critical circuits in the periphery of CMOS memory [1]. Having this kind of configuration has helped in gaining in speed and also reducing the dynamic and static power consumption. The concepts of variation of threshold voltages [2]. The performance of SA's strongly affects both memory access time, and overall memory

power dissipation. As with other ICs today, CMOS memories are required to increase speed, improve capacity and maintain low power dissipation. SA are used to translate small differential voltage to a full logic signal. The design of fast, low-power and robust SA circuits is a challenge, due to the fact that in modern memory designs bit-lines exhibit a significant capacitance, since there is a higher number of cells per bit line, which sets limits in the sensing speed and introduces extra signal delays. This problem can be alleviated when current signals are sensed rather than voltage signals [3], Many current mode SA have been presented in the open literature. The majority of them is based on the cross-coupled transistor topology [4,5]. The conventional current-mirror SA is shown in Figure (1) [6]. The speed can easily accelerated by increasing the operating current. Thus, memories frequently use this type of SA. However, the static current flows through the transistor M5 connected to ground, to accelerate the sense speed needs much power..

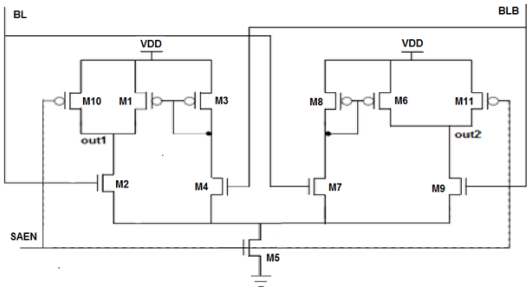

Fig. 1. The current-mirror SA (conventional)

The current controlled latch SA is a second type of current mode SA, see Figure (2). The current flow through M1 and M3 controls the serially connected latch circuit. A small difference between the current through M5 and M6 converts to a large output voltage.

The third type of current mode SA is clamped bit-line SA, see Figure (3). It requires an extra timing signal for operation. It has no provision for stopping the flow of static current, and hence dissipates power even when there is no data activity on the interconnect. To reduce the power in standby mode, adopting a multi-threshold voltage technique reduces the leakage current [7].

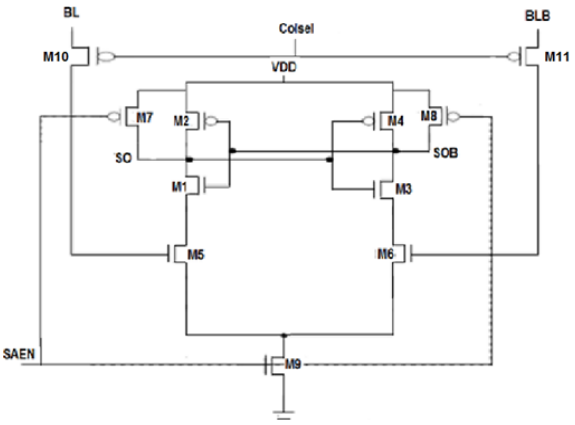

Fig. 2. The current controlled latch SA

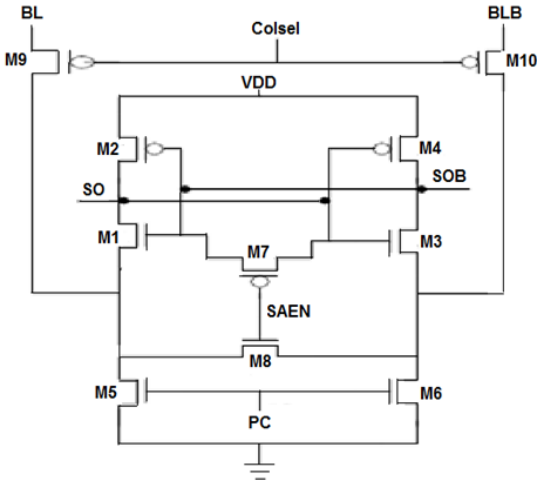

Fig. 3. The clamped bit-line latch SA

Multi-Threshold-Voltage CMOS (MTCMOS)

The multi-threshold-voltage CMOS (MTCMOS) circuit was proposed by inserting high threshold devices in series into low threshold voltage circuitry. Figure (4) shows the schematic of an MTCMOS circuit [8]. A sleep control scheme is introduced for efficient power management.

Two high threshold voltage transistors are used, high threshold voltage PMOS is connected to the power supply, where NMOS is connected to the ground. Due to these transistors a virtual power supply and ground are appeared respectively on the drain terminal nodes of the both transistors. In

the active mode, SL is set low and sleep control high-threshold voltage (MP and MN) are turned on. The virtual supply voltage (V_{DD} and V_{SS}) almost function as real power lines. In the standby mode, SL is set high, MN and MP are turned off and the leakage current is very low. In this only one type of high threshold voltage transistor is enough for leakage control [9].

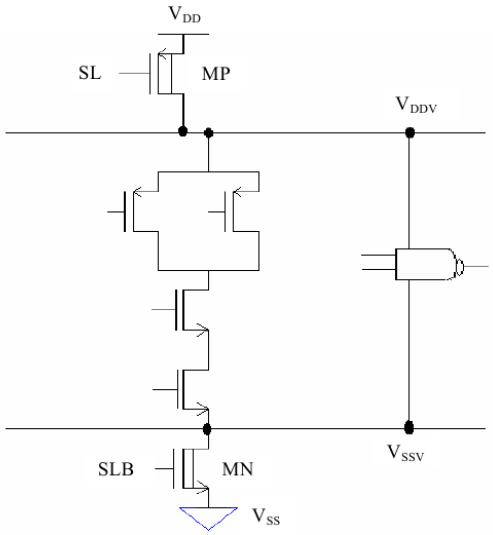

Fig. 4. Multi-threshold CMOS (MTCMOS)

Current Mode Sense Amplifier with MTCMOS Technique

The speed of VLSI chips is increasingly limited by signal delay in long interconnect lines. Major speed and power improvements are possible when using current mode rather than voltage mode signal transporting techniques [10].Moreover, with current mode sensing, reduction in the size of memory cell is another possibility [11]. This designed sense amplifier is based on the current mode approach. The sensing speed is independent of the bit line and data line capacitances and a separated positive feedback technique is employed to give the circuit high speed, low power operation. As the density of memory devices increases, certainly the associated parasitic capacitances also increase. Large capacitive loads cause a major sensing delay in memory devices, so high speed sense amplification of small memory cell signals is the key to achieving a fast access time in SRAM. Conventional sense amplifiers are based on voltage sensing techniques, which are sensitive to parasitic capacitance. A recent approach to designing sense amplifiers employs current sensing techniques. The advantages in term of speed are obvious and very attractive, especially if the supply voltage is low and the memories are large. A current-mode sense amplifier using MTCMOS technology, which gives fast access time and low power consumption, is presented. In addition, it is insensitive to both bit-line and data-line capacitances. The circuit is shown in Figure (5).

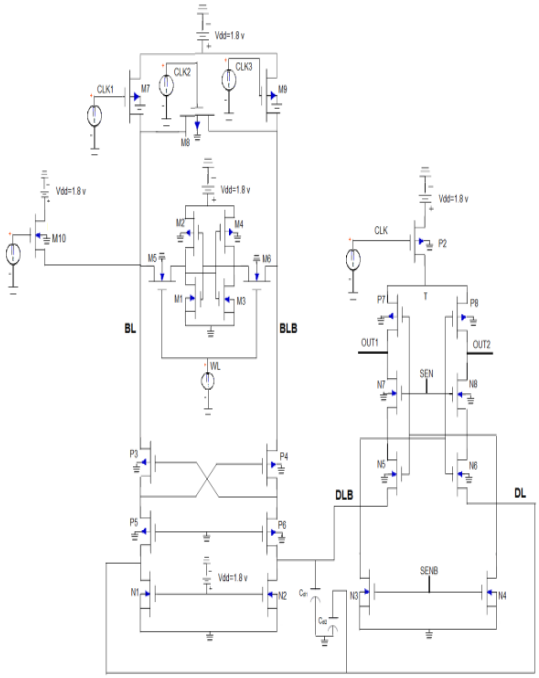

Fig. 5. Current mode sense amplifier with MTCMOS technique

This design is based on the multi threshold voltage CMOS technique. A high threshold voltage PMOS transistor P2 is connected to the power supply which generates a voltage near to supply voltage at the node T. The current through (P3-P6) used in the conventional current sense amplifier is adopted for column sensing. The pre-charge equalizing device is omitted because the current conveyor intrinsically keeps the bit-line at equal potentials once CL is initiated. The N5-N6 and P7-P8 are formed in ways

similar to positive feedback latches. N1 and N2 connect the input nodes and pull down the data-lines close to the ground level. The transistors N7 and N8 are the separating transistors and the transistors N3 and N4 are the equalization transistors [12]. The data-line capacitance are represented by C_{dl1}, C_{dl2} is the column-line selector signals. Due to the low impedance at the input nodes, the current signals at the data-lines are injected to the cross-coupled latch without charging or discharging of the data-line capacitances. Therefore the sensing speed is insensitive to both bit line and data-line capacitances. Transistor aspect ratios are summarized in Table (1).

Table 1. Transistor aspect ratios

Transistor	W/L(μm)
M7-M8-M9	8/0.25
M10	3/0.25
M1-M3	6/0.25
M2-M4	2/0.25
M5-M6	4/0.25
N1-N2	50/0.25
N3-N4	10/0.25
N5-N6	40/0.25
N7-N8	40/0.25
P2	200/0.25
P3-P4	5/0.25
P5-P6	30/0.25
P7-P8	23/0.25

The threshold voltage and voltage supply and capacitor values are provided in Table (2).

Table 2. The threshold voltage and voltage supply and capacitor values

Parameter	value
C_{dl1}-C_{dl2}	0.2fF
Voltage supply	1.8v
Threshold voltage for p2	1.2v
Threshold voltage for all PMOS	0.62v
Threshold voltage for all NMOS	0.43v
Lambda	0.125μm

Simulation Results

The simulation results of the current-mirror sense amplifier (conventional) are shown in Figure (6).

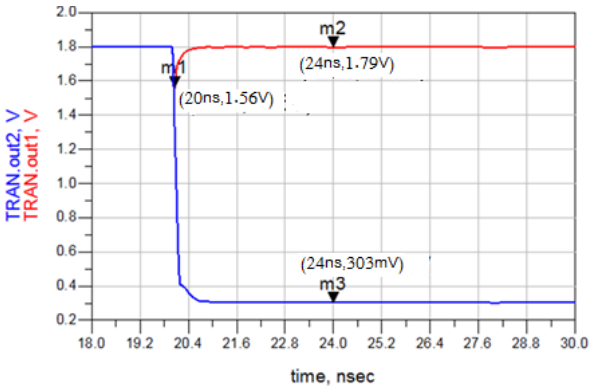

Fig. 6. Output of the current-mirror SA (conventional)

It is observed from the Figure (6) that a delay is 4ns as the SAEN is activated at 20ns .This circuit dissipates 48.68μW power. The simulation results of the current controlled latch sense amplifier are shown in Figure (7).

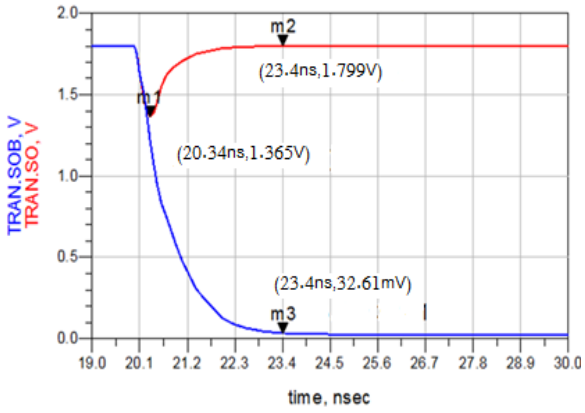

Fig. 7. Output of the current controlled latch SA

It is observed from the Figure (7) that a delay is 3.4ns as the SAEN is activated at 20ns. This circuit dissipates 39.8μW power. The simulation results of the clamped bit-line latch type sense amplifier are shown in Figure(8).

It is observed from the Figure (8) that a delay is 2ns as the SAEN is activated at 20ns. This circuit dissipates 20.4μW power.

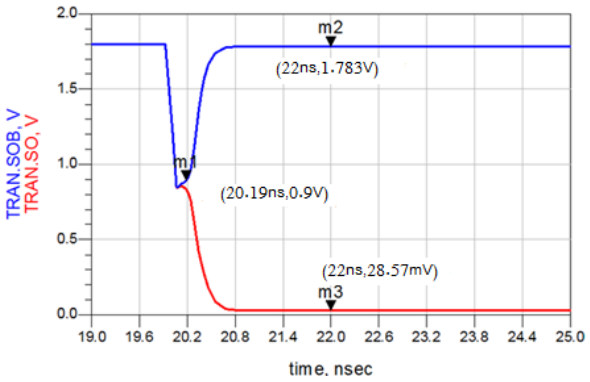

Fig. 8. Output of the clamped bit-line latch type SA

The design of the current mode sense amplifier with MTCMOS technique is based on the MTCMOS technique. In this technique, a high threshold voltage PMOS is connected to the power supply. This PMOS will be turned on only when the circuit required the power supply otherwise it will be off. Power supply is not connected to the circuit when PMOS is off, in this way power dissipation is reduced. It provides a virtual voltage at node T. During the time period 0 to 20ns the circuit is in standby mode. When the sense amplifier is in the standby state, the signal "SENB" is at high-level and the signal "SEN" is at low-level. In this condition, the N3 and N4 are turned on, so the nodes A and B are pulled down to low-level. Hence, the N5 and N6 are at the cut-off state, and the P7 and P8 are operated in the linear region due to their gate voltages being at low level. Since the "SEN" is at low-level, the N7 and N8 are at the cut-off state, which separates the cross coupled latch, therefore, there is no DC current flow in the sense amplifier. During the time period 20 to 180ns the circuit is in active mode. During the read operation, both WL and CL lines are activated. The "SENB" is at low-level, which turns off N3 and N4, and the "SEN" is at high-level to turn on the cross-coupled latch. When a particular memory cell is accessed, a differential current signal appears at the common bit-lines BL and BLB. The current conveyor (P3-P6) transports the differential currents to the data-line. Because the output nodes of the cross-coupled latch are at high-level, at the standby state, there is a large current driven by P7 and P8 and a particular result is obtained at the output. The simulation results are shown in Figure (9).

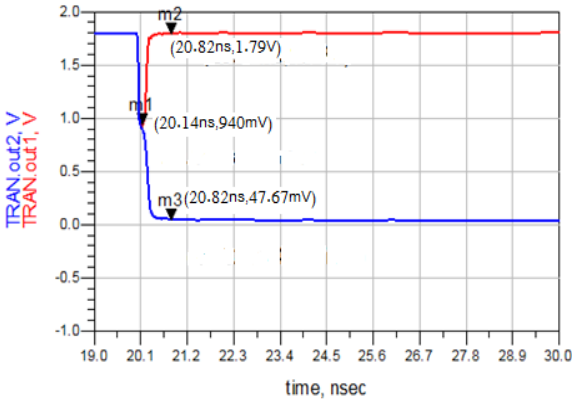

Fig. 9. Output of the current mode SA with MTCMOS technique

It is observed from the Figure (9) that a delay of only 0.82ns is obtained using current mode SA as it is independent of the capacitances. The sense amplifier differentiates the both voltages after a delay of 0.82ns as the WL is activated at 20ns and sense amplifier detects and amplify the signals at 20.82ns. This current mode SA using MTCMOS technique dissipates only 0.395µW power dynamic. When you apply the same circuit but without MTCMOS technique it is observed that a delay is 0.59ns and the power dissipation is 0.549µW this means that this circuit is dissipation more power than the current mode SA with MTCMOS technique. See Figure (10).

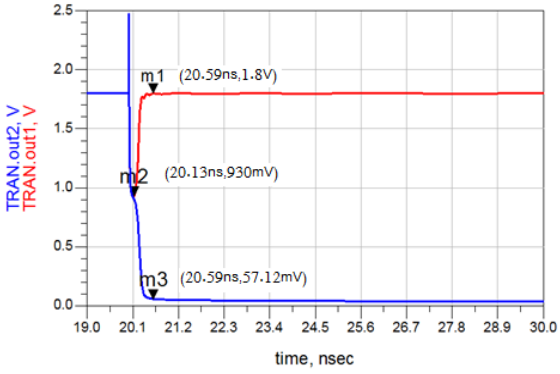

Fig. 10. Output of the current mode SA without MTCMOS technique

The power dissipation of the current mode SA with MTCMOS technique is less compared with the other design and the time delay is less which case high speed sensing for the digital logic.

Table (3) shows the different values of power dissipation and time delay of the current mode sense amplifier.

Table 3. Performance comparison of different sense amplifier

The Circuit	Time Delay	Power Dissipation
The Current Mirror SA	4ns	48.68µW
The Current Controlled Latch SA	3.4ns	39.8µW
The Clamped Bitline Latch SA	2ns	20.4µW
The Current Mode With MTCMOS technique SA	0.82ns	0.395µW

From Table (3) the amount of improvement in power dissipation and time delay are shown by using the current mode with MTCMOS technique Compared with each current mode SA.

Table (4) shows the percentage of improvement of the time delay and the power dissipation in the current mode MTCMOS sense amplifier with respect to other kinds of current mode SA.

Table 4. The percentage of improvement of the time delay and the power dissipation

The Circuit	Percentage improvement for current mode MTCMOS sense amplifier	
	Time delay	Power dissipation
The current mirror SA	387.8%	12224%
The current controlled latch SA	314.6%	9975%
The clamped bit-line latch SA	143.9%	5067%

Conclusion

A low power, high speed sense amplifier using multi-threshold CMOS (MTCMOS) has been proposed. From the simulation results, it is found that the current mode sense amplifier with MTCMOS technique has higher performance compared to the conventional current-mirror sense amplifier, current controlled latch sense amplifier and the clamped bit-line latch type sense amplifier. When the current mode sense amplifier with MTCMOS technique is used for the high speed interconnects, it results in lower power dissipation and has lower time delay. In this paper the (CMOS-0.25µm) technology with supply voltage of 1.8V is used. In this technique the simulation results obtained are 0.82ns time delay and 0.395µW power dissipation. The percentage improvements in time delay and power dissipation of this technique compared to other kinds of sense amplifiers are very special.

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