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Encoding Techniques Based on Reversible Quantum Dot Cellular Automata

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Keywords:
CLK; DSRC; ETC; QCA; MUX.

Highlights:

- *Encode information with line coding for transmission through a channel.*
- *QC gates now incorporate line encoding.*
- *Line encoding was performed using QCA Designer.*

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Abstract: Line encoding technique is essential for data transfer in IoT. It entails encoding the unprocessed bit stream according to designated protocols before transmission. Diverse baseband encoding schemes, including Manchester, Miller, and FM0 codes, are employed to improve communication efficacy. These systems ensure the transmitted signal has zero mean, addressing the issue, of DC balance. These systems ensure the transmitted signal has zero mean, addressing the issue of DC balance. Each encoding strategy should be deployed without missing any of its parameters required. Employing quantum reversible gates can coordinate all encoding techniques, reducing area consumption. The circuit consists of the FM0, Manchester, and Miller encoding to overcome the limitations of current techniques. This derived layout of the FM0 and Manchester coding could promote the DSRC specifications. This paper evaluates the FM0, Manchester, and Miller encoding using QCA Designer, achieving notable reductions in cell count and area. FM0 encoding requires 188 cells, Manchester encoding utilizes 9 cells, and Miller needs 140 cells. The achieved areas (nm^2) were 287512, 24072, and 194969, respectively.

تقنيات التشفير المعتمدة على أتمته الخلايا الكمومية القابلة للعكس

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الخلاصة

يعد تشفير الخط أمرًا حيويًا، خاصة لنقل البيانات، لتصبح جزءًا من إنترنت الأشياء في العالم الطبيعي. حيث إنها طريقة تشفير تدفق البتات الخام واستخدام القواعد قبل إرساله عبر قناة الإرسال. يتم استخدام أنظمة تشفير النطاق الأساسي المختلفة، بما في ذلك رموز مانشستر وميلر وFM0، لتعزيز أداء الاتصالات. من المقدر أن يكون للإشارة المرسلة متوسط صفر لمسألة القوة، والتي يشار إليها عادة باسم توازن التيار المستمر. يجب نشر كل استراتيجية تشفير دون فقدان أي من معلماتها المطلوبة. يمكن أن يؤدي تحسين العمالة إلى استهلاك مساحة كبيرة. نحن نستخدم بوابات كمومية عكسية لتنسيق جميع تقنيات التشفير. تتكون الدائرة من ترميز FM0 ومانشستر وميلر لتتحمل القيود المفروضة على التقنيات الحالية. يمكن لهذا التصميم المشتق لترميز FM0 ومانشستر أن يعزز مواصفات اتصالات مخصصة قصيرة المدى . يتم تقييم إنجاز هذه الورقة باستخدام مصمم QCA. يتطلب بناء FM0 ١٨٨ خلية، وتستخدم مانشستر ٩ خلايا، ويحتاج ميلر إلى ١٤٠. كما أن المساحة المستخدمة للتصميم (nm^2) هي ٢٨٧٥١٢ و٢٤٠٧٢ و١٩٤٩٦٩ على التوالي.

الكلمات الدالة: الساعة، اتصالات مخصصة قصيرة المدى، جمع الرسوم الالكترونية، الاليات الخلوية الكمومية، متعدد.

1.INTRODUCTION

Short-range in nature communication through wireless systems are essential for daily living, such as Wi-Fi, Zigbee, Bluetooth, and RFID protocols, which have revolutionized protection, medical treatment, vehicle communication, and applications for consumers. These forms of technology utilize multiple different physical layer protocols for encoding informational bits [1]. DSRC (Dedicated Short-Range Communication) can allow a single- or two-way communication between devices. DSRC is essentially a form of communication over wireless networks. This product is primarily intended for automotive applications [2]. DSRC has two essential groups: roadside-to-automobile and automobile-to-automobile. In automobile-to-automobile communication, the DSRC transmits and receives signals from one automobile to another for protection and public data purposes. Its automotive-to-roadside DSRC systems focus mainly on smart transportation services, such as electronic toll collection (ETC) devices [3]. Innovative line encoding strategies are crucial for IoT and short-range communication due to their improved bandwidth utilization, which helps save energy while enhancing data security, error recognition, and repair. These strategies contribute to boost equipment life of the battery, lower latency real-world applications, while preserving sender-receiver synchronization through decreasing the total amount of data transmitted. Furthermore, uniform encoding mechanisms stimulate interoperability through different equipment that allows better interaction in growing IoT scenarios [4]. Encoding is the operation of transforming a stream of bits into an appropriate format during data communication. Encoding is present in the physical layer of the OSI architecture. Typical techniques for encoding included FM0, Miller, and Manchester [5], creating increased efficacy and precision. However, this requires a higher frequency clocking [6]. QCA (Quantum Dot Cellular Automata) represents a nanoscale computer device that utilizes tiny quantum dots to demonstrate binary data through electron arrangement. In contrast to standard CMOS (Complementary Metal-Oxide-Semiconductor) technology, that depends upon current movement for logical processes [7], QCA is working on the electrostatic attraction of quantum dots, resulting in significantly reduced the power consumption as well as high-rate processing [8]. In this article, Manchester, Miller, and FM0 code structures were analyzed utilizing QCA Designer tools, including XOR gates, multiplexers, and flip-flops, at the circuit architecture level. This architecture is suitable for tasks that involve switching between multiple encoding strategies. Utilizing distinct circuits for each encoding strategy would need more resources [9]. The work is organized with the following structure: Section II outlines the coding concepts of Manchester, FM0, and Miller encoding. Section III discusses QCA fundamentals. Section IV discusses the QCA Designer technique for simulating the FM0, Manchester, and Miller encoders. Section VI describes the collection of results. Finally, Section VII provides the conclusion. This paper utilizes CLK and A to represent the clock's signal and the data being input, respectively.

2.ENCODING TECHNIQUES

2.1.FM0 Encoding

FM0 has been referred to as bi-stage space encoding, and it is a type of Non-Return-to-Zero code. It also demonstrates signals that are binary in digital systems [10]. Each part allows for a move, with the possibility of an extra move within a bit. Here, the information keeping up is doubled [11]. Obtaining adequate clock data from the information stream eliminates the demand for an extra clock. As a result, transmission demanded fewer cables [12]. Figure 1 demonstrates the FM0 encoding. FM0 coding rules are summarized in the following three guidelines [13]:

1) Given that A is logic-0, there is a change from A to CLK.

2) Given that A is logic-1, there is no valid transition between A and CLK.
3) The change is provided to each one of the FM0 codes, irrespective of the A.

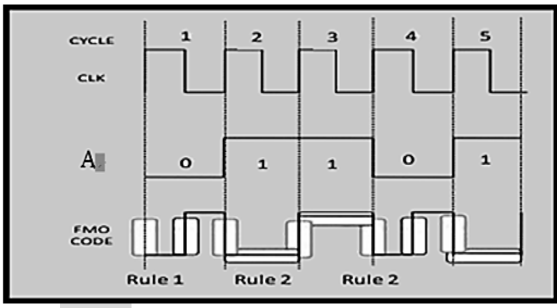

Fig. 1 FM0 Encoding Demonstration

The model's structure requires two D flip-flops to keep the FM0 state code. MUX-1 will transmit either Z(t) or Y(t), depending on the control signal CLK. By employing the formula in Eqs. (1) and (2), Z(t) and Y(t) could be executed easily [14].

$$Z(t) = \overline{Y(t-1)} \quad (1)$$

$$Y(t) = A \oplus \overline{Y(t-1)} \quad (2)$$

2.2. Manchester Encoding

The encoding of Manchester is commonly referred to as phase encoding. It allows for a larger frequency of operation. The encoded Manchester is a famous approach, and it is possibly the most commonly used. Data can be carried in series [6]. The Manchester code is encoded via a process known as XOR between the input data and the clock's timing. The Manchester techniques makes and creates the change between every cycle's centers [15]. Figure 2 illustrates a representation of Manchester coding.

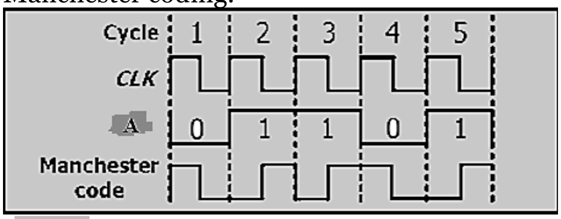

Fig. 2 Manchester Encoding Demonstration.

2.3. Miller Encoding

Miller encode is frequently referred to as delayed encode. It could be employed at higher frequencies of operation and is identical to the Manchester encoder, except for the change occurs in the midst of a period while the bit value is 1. The Miller delay assists in minimizing interference from noise. In Manchester, encoded signals are conveyed under the following set of conditions [16]:

1) The phase inversion happens at the data point '1' representation.
2) The phase shift happens when the logical '1' value follows after the lengthy continuing logic '0' value.

The structure of the model contains a D flip-flop, a T flip-flop, a NOT gate, and an XOR gate [17]. Figure 3 illustrates a representation of Miller coding.

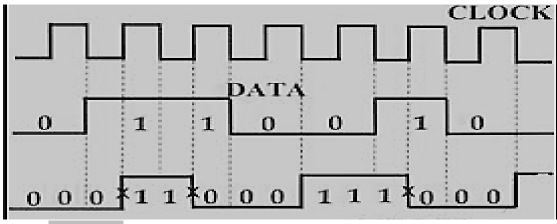

Fig. 3 Miller Encoding Demonstration.

3. QCA FUNDAMENTAL

The primary goal of building a logic circuit is to eliminate wasteful energy consumption. In reversible calculations, data corruption leads to the waste of energy in the form of heat. Quantum gates are innovative logic gates intended for minimizing the loss of energy. The intention is to conserve energy while maintaining the content of information. Implementing circuits with quantum logic could significantly decrease thermal energy waste [18]. This section examined the structural blocks of QCA, covering QCA cells, generalized logic, and gates, specifically in the following sequence: QCA cells, QCA wiring, and majority gates [19].

3.1. QCA Cell

Figure 4 demonstrates a QCA cell, which is a square in form. Every single cell includes a pair of electrons and four transporters, which maintain the flow of electrons. Tunnels transmit electrons, from one transporter to another [20]. The electrons are positioned diagonally in quantum dots to identify cell polarity [21]. Figure 5 illustrates that the electron distribution on the diagonal leads to a pair of distinct state polarizations, established either "0" or "1". The cell having polarization -1 symbolizes binary mode 0, while the cell having polarization +1 symbolizes binary mode 1 [22]. Cell polarization is determined by Eq. (3) [23]. The primary benefits of QCA included smaller circuit terms of size, larger clock frequencies, and less consumption of power [22]. QCA cells have two main structures, which include an inverter and a majority gate [21].

$$\mathcal{P} = \frac{(\mathcal{P}_1 + \mathcal{P}_3) - (\mathcal{P}_2 + \mathcal{P}_3)}{\mathcal{P}_1 + \mathcal{P}_2 + \mathcal{P}_3 + \mathcal{P}_4} \quad (3)$$

where $\mathcal{P}_i$ denotes the electric charge at the i th node.

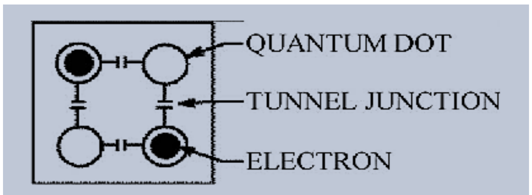

Fig. 4 QCA Cell Description.

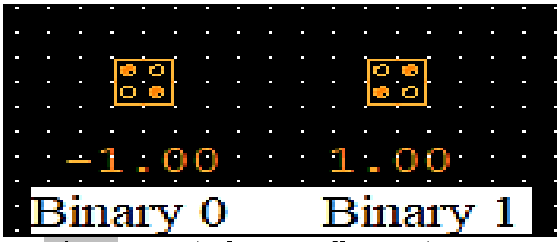

Fig. 5 A Typical QCA Cell Contains Two Polarization Decisions if Binary is Zero or One.

Clocking is one of the most important components of QCA in the field of technology, requiring strict adherence to standards to provide accurate results. Figure 6 depicts the four distinct phases of clocking, each with its unique importance [24]. In the scenario of a switch, cell processes initially start unpolarized and with tiny potential barriers; however, these barriers are raised. In the situation of hold, the barriers are kept high, and every single cell is polarized as when the electrons proceed to the dots that need the least amount of energy, based on the responsible cell [20]. During the release period, the arriving force decreases and leads to electrons to go from a stable to a going situation. During the relaxation period, the receiving force is minimized, allowing electrons to move freely across the cell [24].

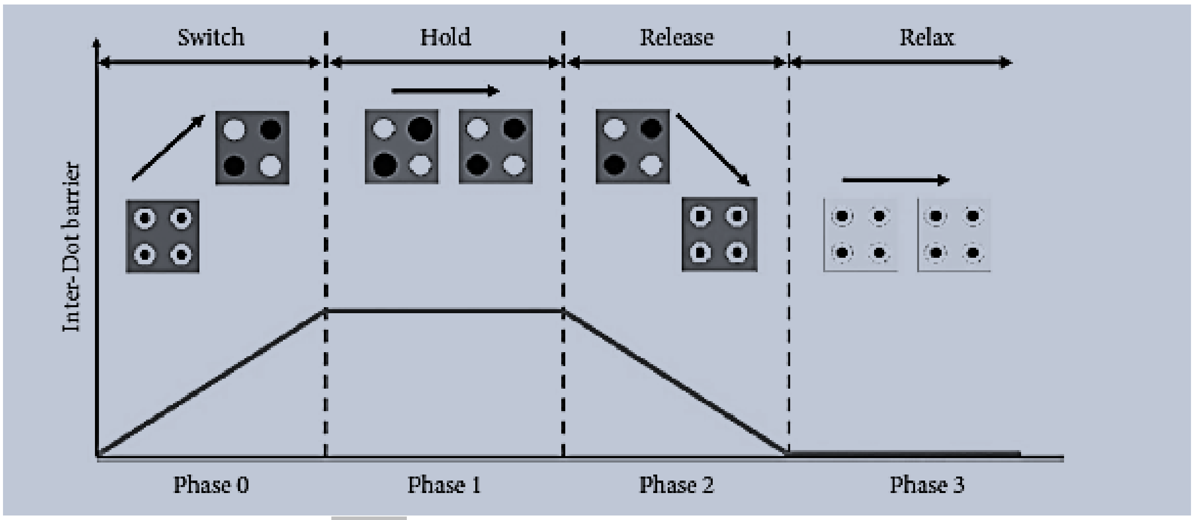

Fig. 6 Clocking employing QCA architecture.

3.2. QCA Wire

The least complex part of QCA is the binary wire, which differs from conventional wires in functionality and layout. Figure 7 depicts the 90-degree wire, considered the most commonly employed and easiest to implement in QCA. This particular kind of wire is composed of an array of QCA cells, arranged either horizontally or vertically. If the input is placed into the initial one-cell, a binary signal passes along the wire through Coulombic repulsion and timing [25].

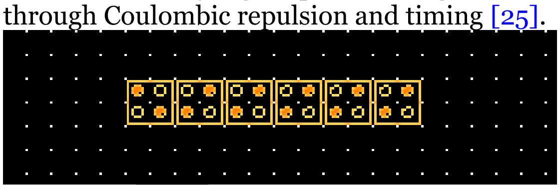

Fig. 7 90-degree wiring.

Figure 8 illustrates employing of a 45-degree wire in QCA. A 45-degree wire permits the simultaneous transfer of both the value in binary and its reversed value, thereby eliminating the need to obtain the latter [26].

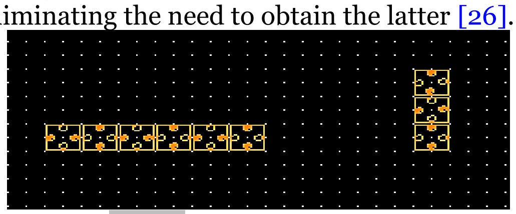

Fig. 8 45-Degree Wiring.

3.3. Majority Gate

In QCA, the standard gate indicates a majority of gates. This gate consists of three inputs, a single output, and a device cell. The gate with this name was designated after its ability to choose across three inputs and send the most polarized output. The device cell required most of the polarity to reduce Coulombic repulsion around electrons via three inputs [25]. This gate could construct basic logical gates, including AND and OR, simply by setting one of its inputs to 0 or 1 [26]. QCA has resulted in two kinds of majority gates, as shown in Fig. 9. The typical equation for this gate is as outlined below [27]:

$$\mathcal{M}(\mathcal{A},\mathcal{B},\mathcal{C}) = \mathcal{AB} + \mathcal{AC} + \mathcal{BC} \quad (4)$$

where $\mathcal{A}, \mathcal{B}, and\ \mathcal{C}$ are input. Eqs. (5) and (6) demonstrate how NAND and NOR gates can be built via minority gates. Figure 10 illustrates a representation of a minority gate [28].

$$\begin{aligned}\mathcal{M}(\mathcal{A},\mathcal{B},0) &= \grave{\mathcal{A}}\grave{\mathcal{B}} + \grave{\mathcal{A}}\grave{\mathcal{C}} + \grave{\mathcal{B}}\grave{\mathcal{C}} \\ &= \grave{\mathcal{A}}\grave{\mathcal{B}} + \grave{\mathcal{A}}(1) + \grave{\mathcal{B}}(1) \\ &= (\grave{\mathcal{A}} + \grave{\mathcal{B}}) = \overline{(\mathcal{AB})} \quad (5)\end{aligned}$$

$$\begin{aligned}\mathcal{M}(\mathcal{A},\mathcal{B},1) &= \grave{\mathcal{A}}\grave{\mathcal{B}} + \grave{\mathcal{A}}\grave{\mathcal{C}} + \grave{\mathcal{B}}\grave{\mathcal{C}} \\ &= \grave{\mathcal{A}}\grave{\mathcal{B}} + \grave{\mathcal{A}}(0) + \grave{\mathcal{B}}(0) \\ &= (\grave{\mathcal{A}}\grave{\mathcal{B}}) = \overline{(\mathcal{A} + \mathcal{B})} \quad (6)\end{aligned}$$

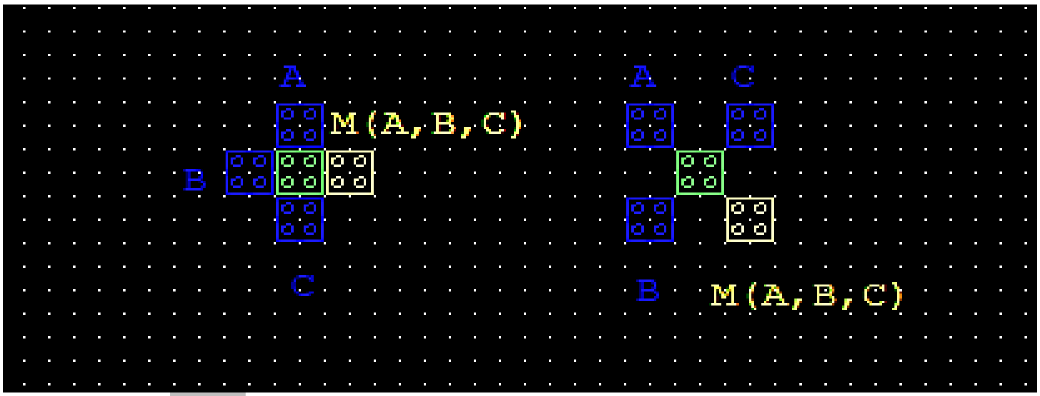

Fig. 9 Majority Gate in QCA: Right) Normal, Left) Rotated.

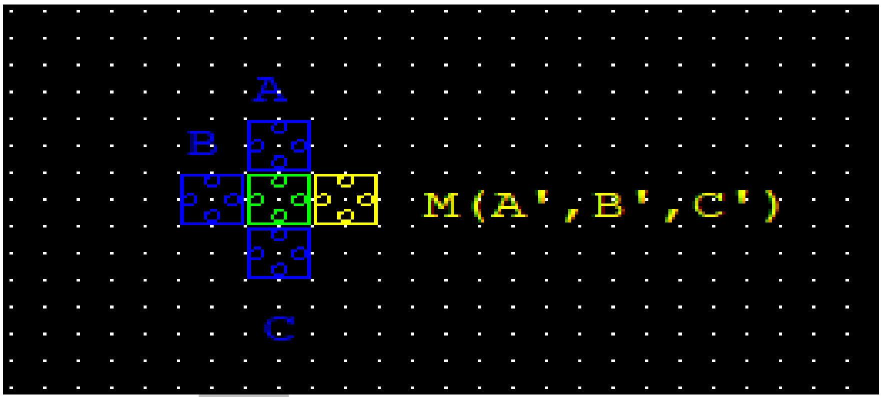

Fig. 10 Majority Gate, a Different Shape.

4.ENCODING TECHNIQUES SIMULATION

The FM0 component comprises a pair of D-flip-flops (DFFs) for preserving the state code, one Mux (2×1) for choosing logics A(t) and B(t), utilizing the clock as a selecting line, and a Not gate. Finally, the Mux with an option is utilized to select the kind of encoding from FM0. If mode = 0, the FM0 code will be chosen, as shown in Fig. 11 [29]. Figure 12 demonstrates how the FM0 encoding was implemented in QCA Designer.

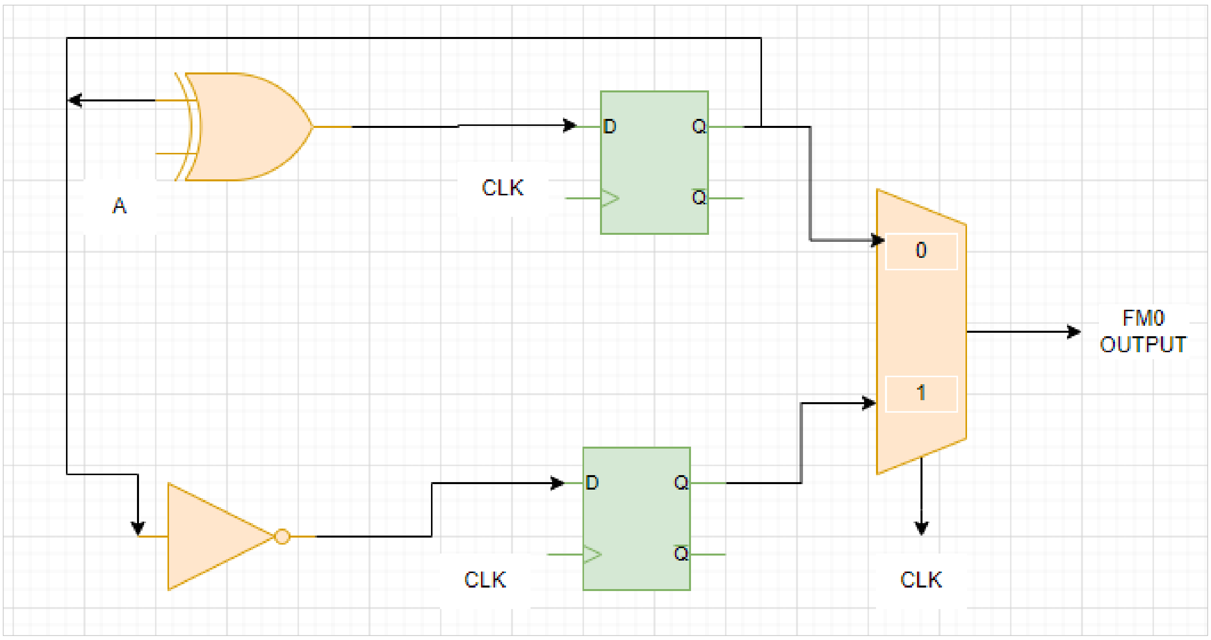

Fig. 11 FM0 Structure Circuit.

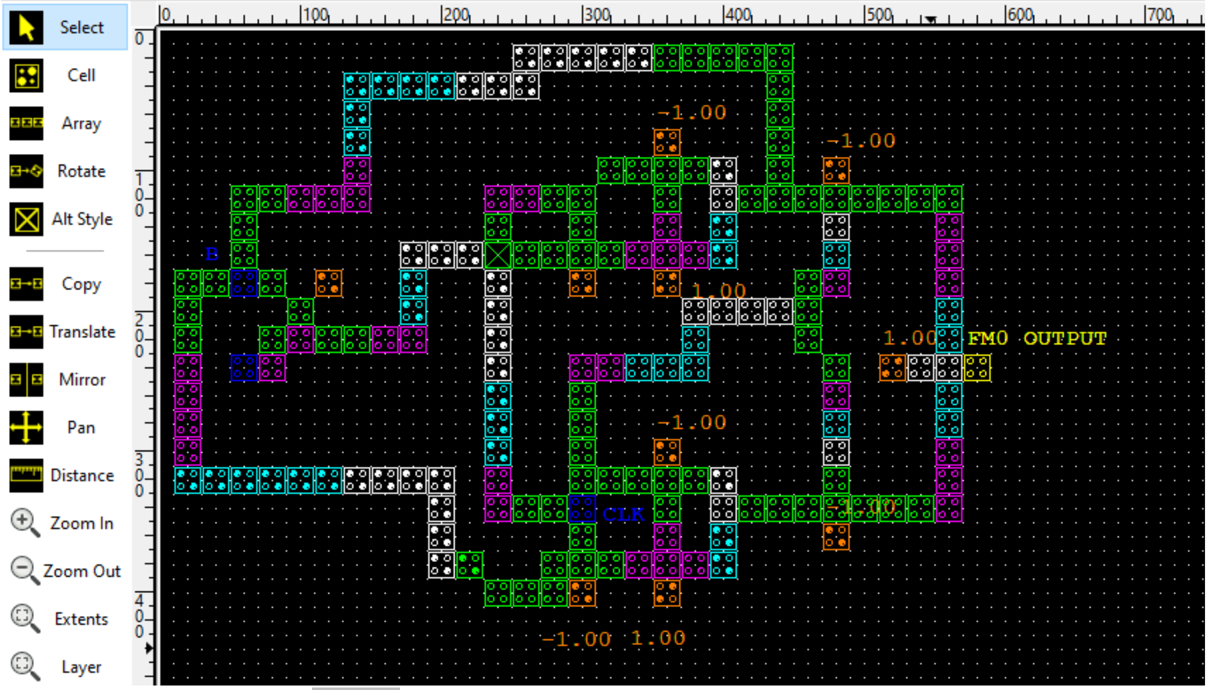

Fig. 12 QCA Emulated FM0 Circuit Architecture.

Manchester encoding is a method of XORing data in binary format with clock pulses of Tb bit length. Figure 13 depicts the Manchester layout. The Manchester code's pulse width doubles to match Tb when the values of the data transfer from 0 to 1 or 1 to 0. Figure 14 demonstrates how the Manchester encoding was implemented in QCA Designer.

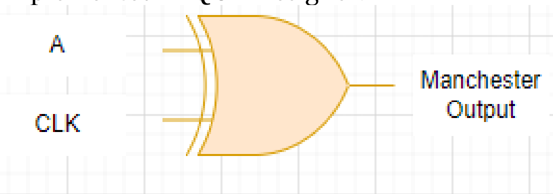

Fig. 13 Manchester Structure Circuit.

Fig. 14 QCA Emulated Manchester Circuit Architecture.

The Miller components consist of a D flip-flop, a T flip-flop, a NOT gate, and an XOR gate. Where both inputs are A and CLK, and the outcome is a Miller result, illustrated in Fig. 15. Figure 16 demonstrates the way that the Miller encoding has been implemented in QCA.

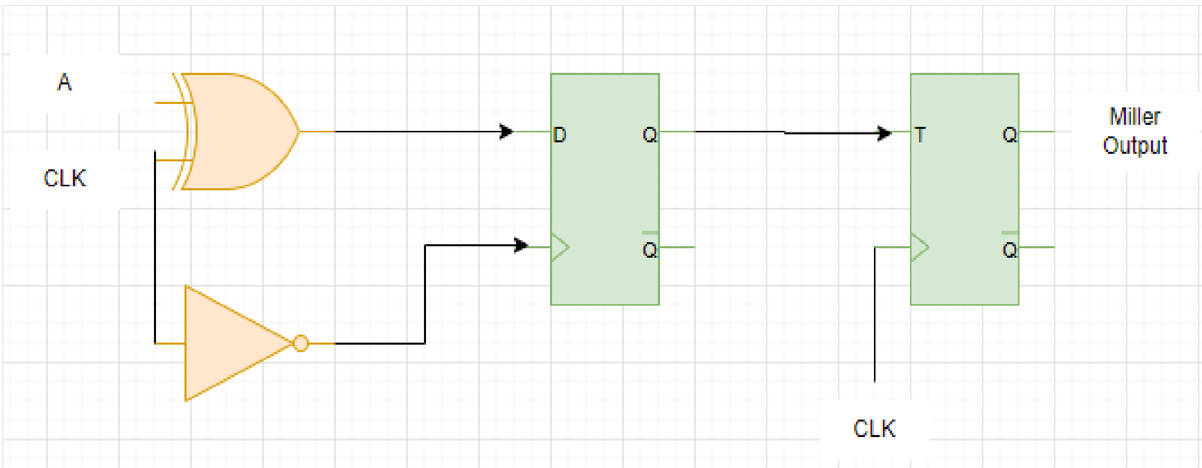

Fig. 15 QCA emulated Miller circuit architecture.

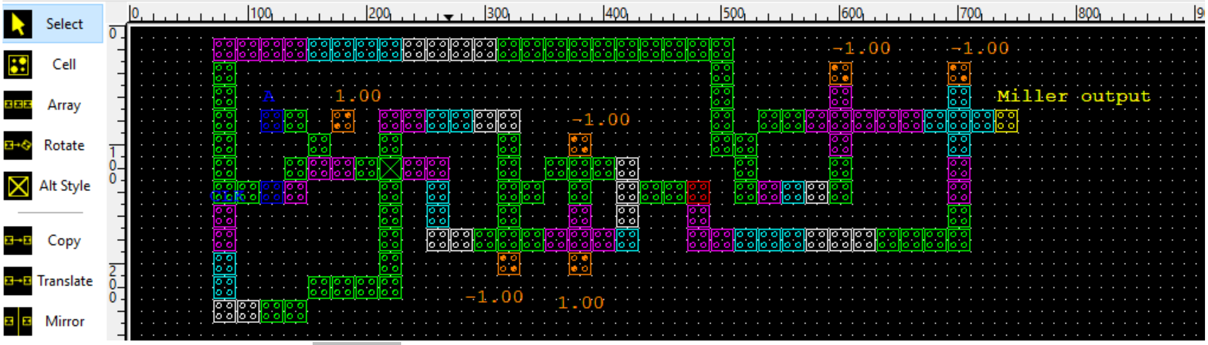

Fig. 16 QCA emulated Miller circuit architecture.

5.RESULT ANALYSIS

QCA Designer, a flexible simulation tool for QCA circuits, was employed to simulate FM0, Manchester, and Miller encodings. The Bi-stable Approximation has been utilized to emulate the circuit that was suggested with the following settings: The cell size was 18 nm, there were 128000 samples, the convergence tolerance was 0.001000, the effective radius was 65.000000 nm, the relative permittivity was 12.900000, the clock high was 9.800000e^{-022} J, the clock low was 3.800000e^{-023}J, the clock shift was 0, the clock magnitude factor was 2.000000, the layer separation was 11.500000, and the maximum number of iterations per sample was 100. The majority of the settings stated here have been set to the factory defaults for Bi-stable Approximation. Figures 12, 14, and 16 illustrate the circuit layouts for FM0, Manchester, and Miller. The input cells are indicated by A and CLK, and the output cells are FM0, Manchester, and Miller. The pair of polarizations, P = +1 and P = -1, was indicated by 1 and -1, respectively. Figures 17, 18, and 19 depict both the input and output shapes of the proposed circuit in QCA Designer. Table 1 displays the various characteristics of the suggested encoding circuit. Table 1 clearly shows that QCA innovation enables a more integrated manufacturing model than CMOS technology. Table 2 compares the suggested technique to the currently available technique. QCA architecture has a larger area effectiveness than CMOS architecture.

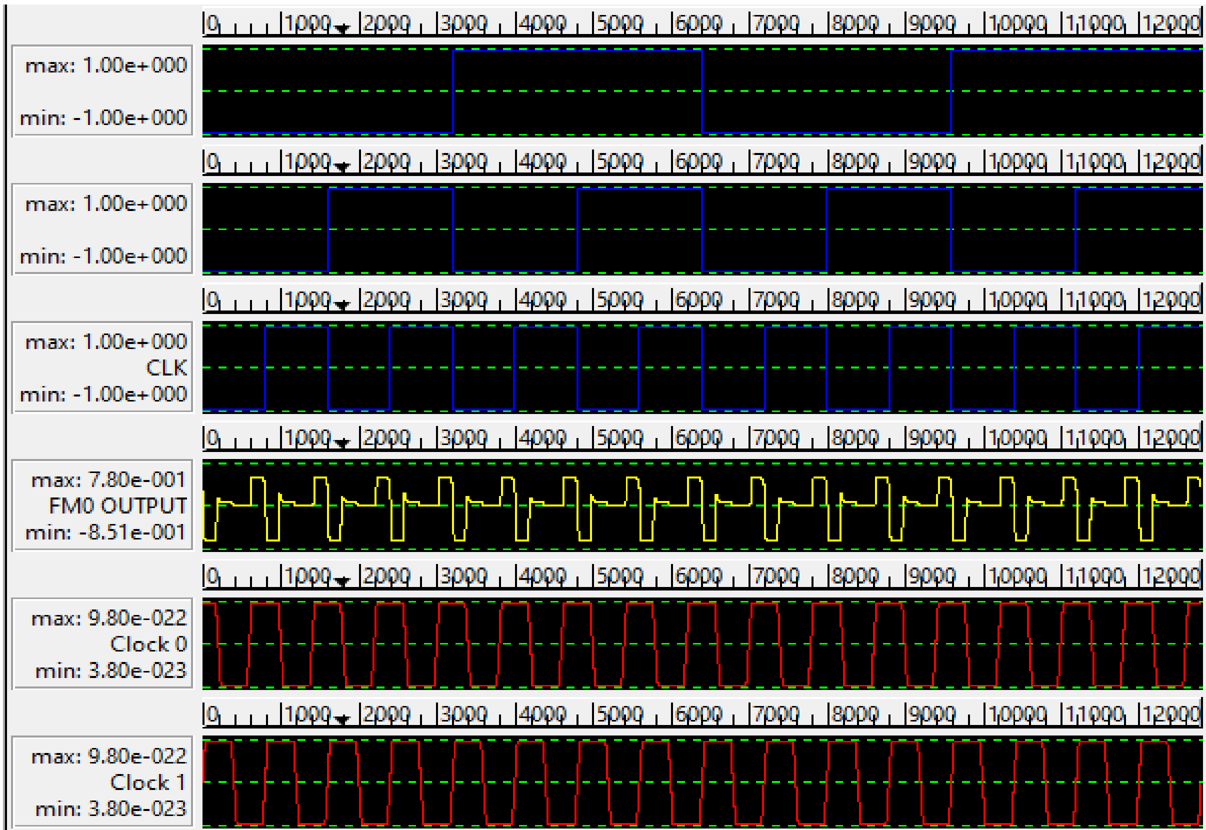

Fig. 17 FM0 Encoding Output Produced by QCA.

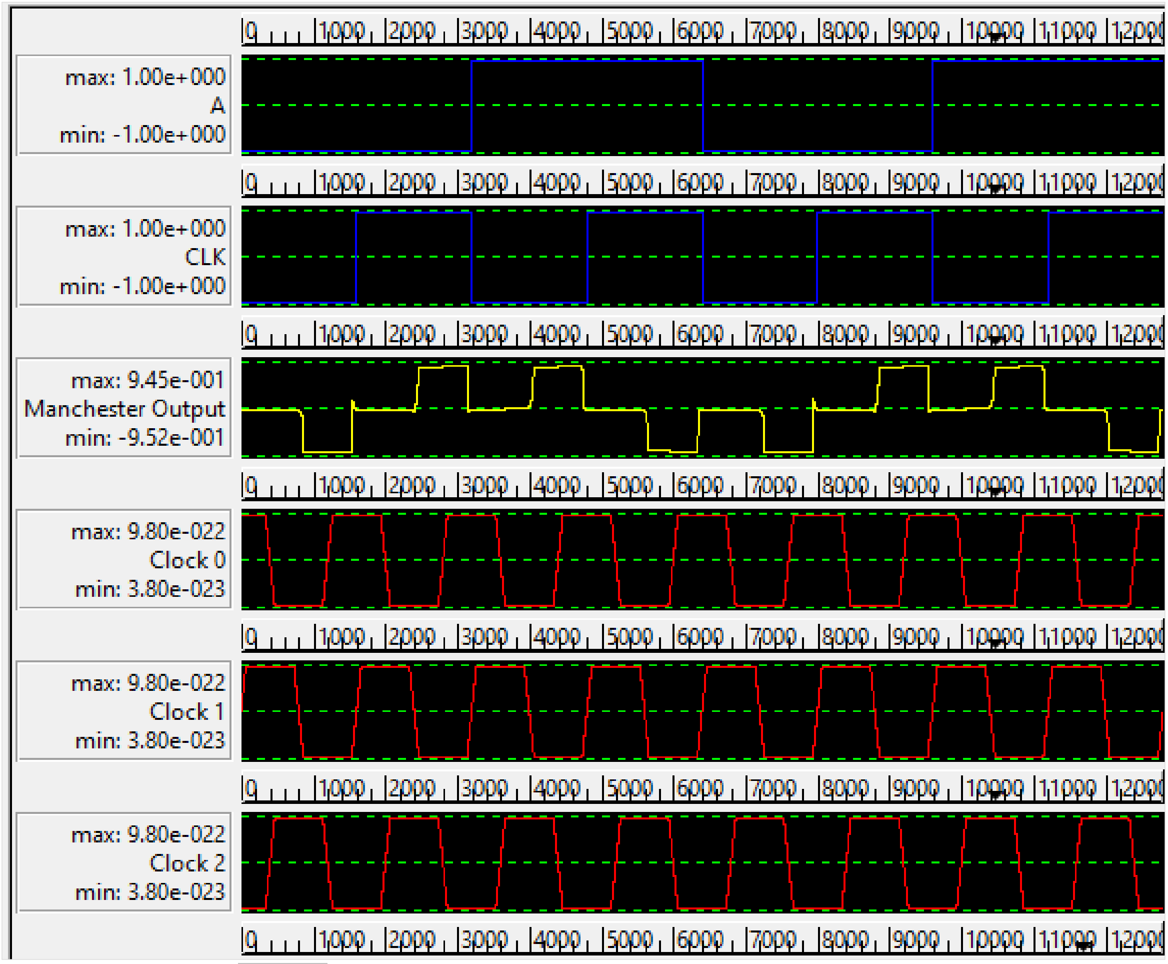

Fig. 18 Manchester Encoding Output Obtained from QCA.

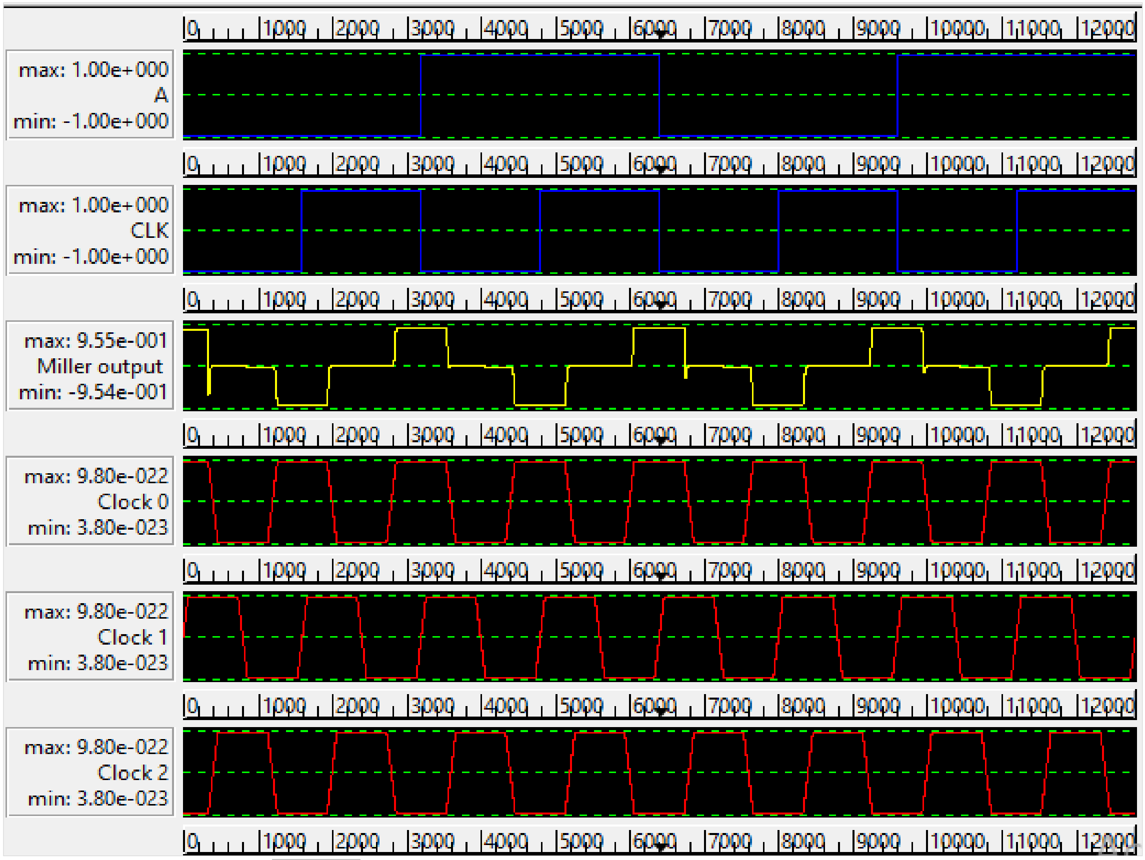

Fig. 19 Miler Encoding Output Generated by QCA.

Table 1 Performance Evaluation of the Suggested Encoding Circuit.

The Variables	FM0	Manchester	Miller
The total number of cells	188	9	140
The delay in time (clock cycle)	0.0013	0.0014	0.00295
Completed area in QCA (nm^2)	287512	24072	194969
Quantum Price (Area * $Delay^2$)	0.4859	0.04718	1.69671

Table 2 A Comparison between the Suggested Technique and the Currently Existing Technique.

Ref.	Technique Used	Encoding Techniques type	Architecture	Delay
[8]	SOLS	FM0+Machester	CMOS	1.754
[9]	SOLS	FM0+Machester	CMOS	3.526+5.753
[16]	SOLS	FM0/Manchester +FM0/Miller	CMOS	2.498+1.535
[27]	SOLS	FM0/Machester+Differential Manchester	CMOS	5.776
Suggested	-----	FM0+Machester+Miller	Quantum (Reversible)	0.0013+0.0014+0.00295

6.CONCLUSIONS

This paper presents the implementation of QCA Designer employing FM0, Manchester, and Miller encodings, which are significantly tiny than CMOS and in tremendous demand in the market for semiconductors. These suggested QCA logic architectures have been constructed with minimal cell count, overall area, and QCA price. FM0 encoding required 188 cells, Manchester needs 9 cells, and Miller utilized 140 cells. Compared with the classic architecture, this strategy mitigated delay and enhanced circuit hardware consumption. The planned improvements involve constructing a differential Manchester encoding and error-correcting strategy for QCA.

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