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Optimization of Eye Diagram Based on Adaptive Decision Feedback Equalizer for High Speed Digital System

Amenah. I. Kanaan
Electronics Engineering College, Electronic Department, Mosul University, Mosul, Iraq

Abstract

Eye diagram used in a lot of radio and telecommunication application, but it can also be used in digital signal integrity. This kind of analysis is a common indicator of performance in digital transmission systems. As integration density and data rates increase, dispersive losses, reflections and crosstalk can severely degrade signal integrity. Fortunately, these effects are linear processes. Accordingly, simple, on-chip signal processing techniques can compensate for them. In this paper we introduce an approach to improve eye diagram for data transmission that indicate the signal strength by using adaptive Decision Feedback Equalizer (DFE) in receiver circuits of digital system. The simulation results are presented to validate the efficiency of the proposed method.

Keywords: Eye diagram, FIR filter, Decision Feedback Equalize (DEF).

تحسين مخطط العين القائم على أساس استخدام مساوي القرار للتغذية الخلفية المتكيف للأنظمة الرقمية العالية السرعة

الخلاصة

يستخدم مخطط العين بشكل كبير في تطبيقات الأنظمة الراديوية وأنظمة الاتصال عن بعد، و أيضا ممكن أن تستخدم من اجل معرفة مدي سلامة الإشارة الرقمية. هذا النوع من التحليل هو مؤشر عام لأداء أنظمة الإرسال الرقمية مع زيادة معدلات البيانات وكثافة توحيدها فان خسائر التوزيع، الانعكاسات والتشويش على خطوط الاتصال يمكن أن تقلل بشكل كبير من سلامة الإشارة الرقمية المرسلة. لحسن الحظ فان هذه التأثيرات هي عمليات خطية لذلك فان تقنيات معالجة الإشارة ممكن أن تعوض عن هذه الخسائر. في هذا البحث قدمنا طريقة لتحسين مخطط العين للبيانات المرسلة والتي تبين في نفس الوقت قوة الإشارة عن طريق استخدام مساوي القرار للتغذية الخلفية في دوائر الاستقبال للأنظمة الرقمية. نتائج التمثيل بالحاسبة استعرضت لتثبت كفاءة الطريقة المقترحة.

الكلمات الدالة: مخطط العين ، مساوي القرار للتغذية الخلفية، فلتر استجابة النبضة المحدودة.

Introduction

Modern technology has been moving toward higher speeds and smaller form factors. Some non-ideal effects previously considered to be negligible in printed circuit boards (PCBs) become critical design challenges for meeting the signal/power integrity (SI/PI) and electromagnetic interference (EMI) requirements. Among them, one important effect is the frequency dependent losses of transmission line mainly attributed to the finite conductivity of imperfect conductors and the naturally electric polarization of dielectric materials. It might cause serious intersymbol interference (ISI) problems, leading to the occurrence of poor eye diagram and even false switching of logic gates. This must be taken into account carefully, especially for the digital systems with long-distance data transmission inside [1].

With the continued increase in speeds of digital systems, designers and researchers are faced with problems containing an increased number of unknowns. Analysis and modeling issues that can be neglected at lower speeds become significant at higher speeds and must be considered in the design of the system. Modern technology has been moving toward higher data rates, intersymbol interference (ISI) has a significant impact on signal integrity and timing, and thus the occurrence of poor eye diagram. ISI is defined as one symbol interfering with subsequent symbol and is usually resulted from channel impairments such as frequency dependent losses and multiple reflections[2]. As integration density and data rates increase, dispersive losses, reflections and crosstalk can severely degrade signal integrity. Fortunately, these effects are linear processes. Accordingly, simple, on-chip signal processing techniques can compensate for them. This is the basic idea behind equalization as shown in Figure (1). An ideal transmission channel would in all cases deliver a delayed version of the input signal $v_{in}(t)$ from the driver without distortion to the receiver, i.e. $v_{out}(t) = v_{in}(t - td)$, where td is the propagation delay across the channel. Equivalently, an ideal channel would have a frequency response of $e{-}j^{\omega td} I$, where $j = \sqrt{-1}$ and I is the identity matrix whose size is the number of input signals. If an equalizing filter has a transfer function that equals the inverse of the transfer function of the channel, then the concatenation of the equalizer and the channel will have a flat frequency and phase response. However, practical constraints such as power and limited switching time motivate studying optimal equalizing filter design under practical constraints.

Channel equalization can be performed by the transmitter, as shown in Figure(1), preceding the actual channel driver. Transmitters that utilize equalizing filters are called pre-distorting transmitters. Pre-distorting equalizers are commonly realized as finite impulse response (FIR) digital filters. While infinite impulse response (IIR) filters can be more flexible than FIR filters, they are generally not used for high data rate transmission because of the difficulty of calculating the IIR recurrence (i.e. feedback) at very high rates. The inputs to the equalizing FIR filters are the present and past transmitted symbols. The output of the FIR filter is a weighted sum of these symbols. The length of the filter depends on the number of symbols that affect the response of the channel to the current symbol. The filter coefficients depend on the channel characteristics [3]. In this paper we introduce an approach to improve eye diagram for data transmission that indicate the signal strength by using adaptive Decision Feedback Equalizer (DFE) in receiver circuits of digital system. DFE uses desicion feedback to cancel the interferfence from symbols which have already have been detected.

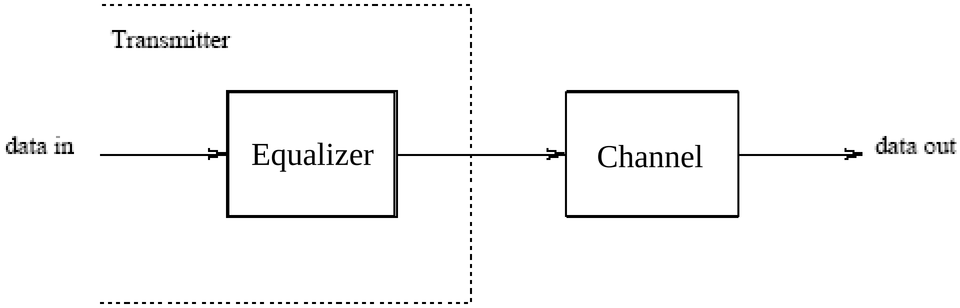


Fig.1. Block diagram of an equalized transmission channel

Related Works

Many reserchs have been presente in this feild as: Yung-Shou Cheng, Yen-Cheng Lai, and Ruey-Beei Wu in 2010 proposed a systematic methodology based on arbitrary step response to determine the tap setting of multi-tap finite impulse response (FIR) filter for best eye diagram improvement. The required tap number and the optimal tap coefficient are determined according to the compensation efficiency and hence the ultimate performance of FIR filter is evaluated. Eventually, the compensation results for two specific 5Gbps signaling system, which include significant effects of losses and multiple reflections, are demonstrated in this paper to validate the optimization method [2]. In 2011, Yung-Shou Cheng, and Ruey-Beei Wu introduced a new design algorithm to directly optimize the eye diagram using finite impulse response (FIR) filter as transmitter pre- emphasis to counteract the inter-symbol interference in the high speed data transmission. the optimal set of the tap coefficients and tap numbers are determined by direct search method according to the required specifications on eye mask for different applications [4]. In the same year, Mihai Daraban, and Dan Pitica showed that the eye diagram can be used in analyzing crosstalk problem which appears on a parallel communication bus implemented on PCBs, by using SPICE simulator and Matlab code implementation [5]. So on the same year, B. Ševčík, L. Brančík, and M. Kubíček presented transmitter pre-emphasis techniques to overcome high- slope losses of printed circuit board (PCB) with higher order transfer function used in high speed serial link design. The pre-emphasis technique based on pulse width modulation using timing resolution instead of amplitude resolution to adjust the filter transfer function and then applied to channel with high order function [6].

Undesired RF Communication Channel Effects– loss and Resonance

Nowadays, multi-gigabit signals are transmitted between transmitter and receiver through long channel. The most significant effect, which degrades the signal integrity, mainly comes from the unwanted parasitic loss and capacitance in the channel. The loss components didn't affect signal integrity seriously when the frequency was much less than a single gigabit per second. However, as the operation frequency becomes gigabit range, the loss effects limit the bandwidth of the high-frequency gain resulting in distortion of the signal. Generally, the channel loss results from two kinds of losses; dielectric loss '*ad*' and conductor loss '*ac*'. Dielectric loss is the loss of current by the leakage from signal line to ground through dielectric substrate. As every dielectric material has its loss tangent (tan δ), and the dielectric loss is dependent on the value of loss tangent as expressed in Equation (1) [7].

$$\propto_d = \frac{w\sqrt{\mu\varepsilon}\,tan\delta}{2} \qquad \text{.............(1)}$$

The dielectric loss is proportional to the frequency as frequency goes higher, the signal can propagate through the conductor within limited skin depth. For example, 1 GHz signal can propagate through the conductor line within 2 μm depth. The conductor loss in the microstrip structure is also expressed in Equation (2). The conductor loss is proportional to the root square of the frequency.

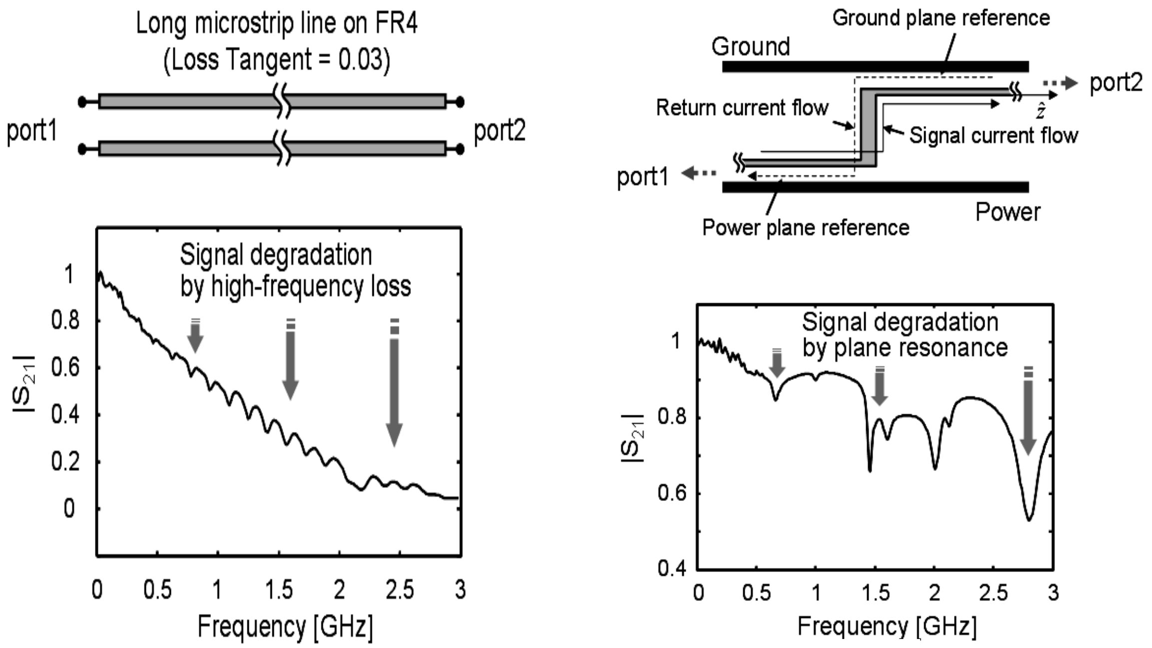
$$\alpha_c = \frac{\sqrt{\omega\mu_o/2\sigma}}{Z_{o\omega}} \qquad \text{.............(2)}$$

If we investigate the dielectric loss and conductor loss, both of them are dependent on the frequency. The higher the frequency of the signal is, the more magnitude of the signal they degrade. Figure (2a) shows the measured S21 parameter through a long microstrip line. The measured S21 parameter along a signal trace with reference change is depicted in Figure (2b).

It is noticed that the insertion loss is quite high at the resonant frequencies. As a result, the losses and resonance reduce some component of the signal, and cause significant ISI. ISI is caused by amplitude attenuation and group-delay distortion. The impedance between a pair of planes is very high at resonant frequencies, which is determined by the geometry of the planes in Equation (3).

$$f_{mn} = \frac{1}{2\sqrt{\mu\varepsilon}}\sqrt{\left(\frac{m}{a}\right)^2+\left(\frac{n}{b}\right)^2} \quad \text{………… (3)}$$

Where (m, n) represents the mode number at a resonant frequency in a pair of rectangular planes with size of (a× b) [8].



(a) **(b)**

Fig. 2. Undesired channel effects (a) frequency dependent channel loss (b) resonance coupled from reference planes

Optimization Principle for FIR Filters Equalizer

For high speed digital signal systems, signal quality will suffer from the reflections caused by impedance discontinuity and attenuation due to frequency dependent losses. These non ideal effects usually result in significant ISI problem. Using the FIR filter for pre-emphasis is a popular technique to eliminate the impact of ISI. Figure (3) depicts a block diagram of the multi tap FIR filter. The output signal of the FIR filter is represented as:

$$y(t) = \sum_{i=0}^{N} b_i . x(t - i.T_d) \quad \text{……..…….(4)}$$

Where bi (i=0, 1, 2,….., N) are the tap coefficients, Thus the set of tap coefficient is defined as

$$[bi] = [b0, b1,……., bN] \quad \text{……..……..(5)}$$

N is the total tap number, and the delay per tap Td is 1 unit interval (UI). The filter response can be adjusted by controlling the tap number and coefficients [2].

To evaluate the compensation efficiency, eye diagram is a very helpful metric of intuitively and quickly assessing the system performance with pre-emphasis. Figure (4) depicts a typical eye diagram with timing jitter (tJ) and voltage noise (VNoise).The height and width of eye diagram are two key parameters to judge the quality of eye diagram.

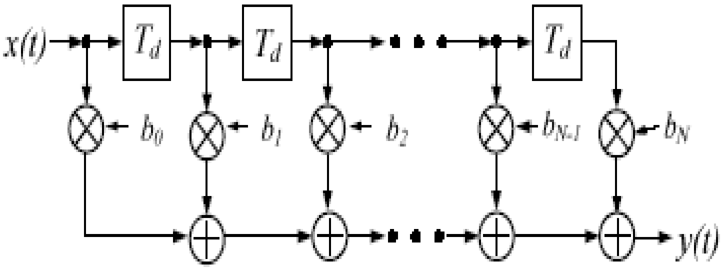


Fig. 3. FIR filter pre-emphasis with N taps

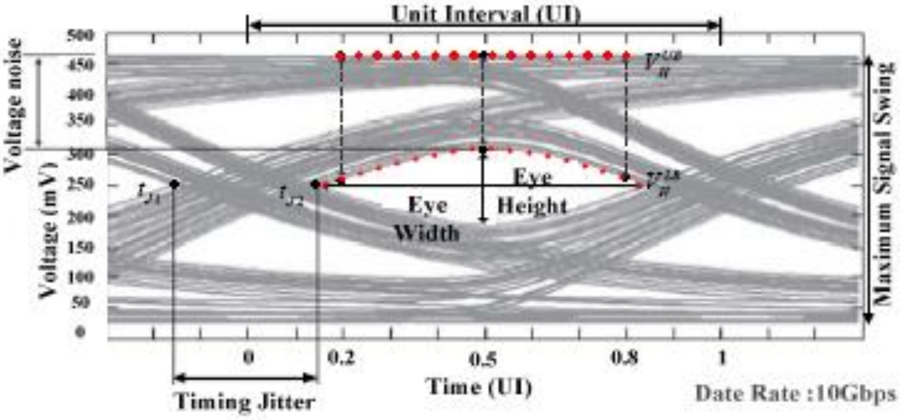


Fig. 4. Typical representation of eye diagram with timing jitter and voltage noise

The two key parameters, which estimate the quality of the eye diagram, that is, eye width and height, can be determined by the amounts of TJ and Vvar , respectively. Due to the symmetry of the eye diagram, the timing jitters

TJ = tJ 2 − tJ 1 …....…. (6)

is defined as the time difference between the earliest and last rising edges cross the threshold voltage Vth.

$$V_{var} = V_H^{ub} - V_H^{lb} \quad \text{……….. (7)}$$

The voltage variation is defined as the voltage difference between the upper and lower bounds at the 1-state. To maximize eye height, the tap coefficients should be chosen to minimize the voltage variation in Equation (8), or equivalently, to make the ratio of V_H^{ub} to V_H^{lb} close to unity [4].

Therefore, it is arguable to select the objective function for the optimized FIR filter design by

$$obj(h[i]) = \max\left(V_H^{lb} / V_H^{Uub}\right)$$
$$as\ obj(h[i] \leq 1)$$

……... (8)

Where h[i] denote the sequence of tap coefficients bi as follows

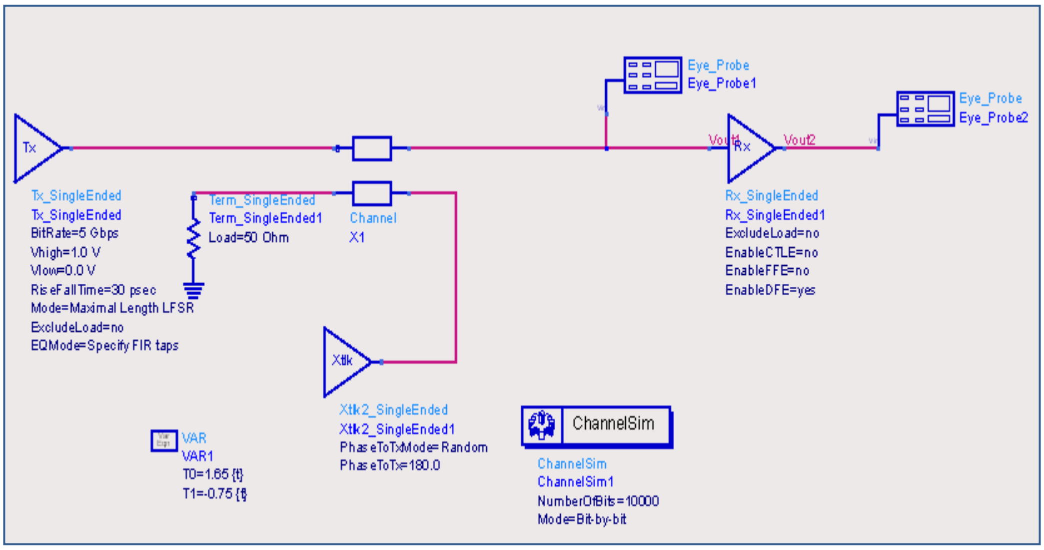
h[i]=[b0,b1,…..,bi] for i=0 to N ………..(9)

As the maximum value of the ratio of V_H^{lb} to V_H^{ub} be found over the range of h[i], the associated tap coefficients are the optimal results.

When inter-symbol interference is present it affects each bit transmitted and so we can no longer tell with precision which bit period we analyze. The eye diagram it imposes an opening which ideal it is equal with the bit period. Closing of the opening of the eye it means that there are transitions that generate errors in the signal. The horizontal width of the cross-over region that separates eye opening is a measure of the jitter. A direct consequence of frequency-dependent lossy lines and an indirect measure of the ISI and crosstalk is the collapse of the opening of the eye. As a rule the collapse of the eye diagram is produced by frequency-dependent lossy line, inter-symbol interference and crosstalk, mean while the widening of the crossover region is given by jitter [5].

Proposed Method and Result

Simulate block diagram of transmission system and the receiver is depicted in Figure (5), which mainly consists of a TX incorporated with FIR filter pre-emphasis, a RX, and a single ended microstrip line with characteristic impedance *Z*0 between them. Using the advanced design system (ADS 2009) simulator properties which include signal integrity analysis, channel simulator to eliminate bit errors and improve eye closure and S-parameter simulator, we build the simulated system inserting FIR filter as a equalizer circuit in the TX and indicate the electrical characteristic of the transmitter.



Tx_SingleEnded
Tx_SingleEnded
BitRate=5 Gbps
Vhigh=1.0 V
Vlow=0.0 V
RiseFallTime=30 psec
Mode=Maximal Length LFSR
ExcludeLoad=no
EQMode=Specify FIR taps

Load=50 Ohm

T0=1.65 {t}
T1=-0.75 {t}

Xtlk2_SingleEnded
Xtlk2_SingleEnded1
PhaseToTxMode=Random
PhaseToTx=180.0

ChannelSim
ChannelSim1
NumberOfBits=10000
Mode=Bit-by-bit

Rx_SingleEnded
Rx_SingleEnded1
ExcludeLoad=no
EnableCTLE=no
EnableFFE=no
EnableDFE=yes

Fig. 5. Simulate block diagram of transmission system and the receiver

Depending on the value of R_S, the cases of under and overdriven transmission lines would be discussed further. In the third case, the transmission line system with matched terminations ($R_S = R_L = R_0$) would be considered to further discuss the lossy effect in long transmission line. In this section, the computation time is for a Core 2dual 2GHz processor with 1GB of RAM.

The bus was analyzed in an Advanced Design System (ADS2009) program that is able to simulate the effects of a PWB. At first were set the parameters of the layers that make up the two side board. The copper on the top and bottom was set to have a thickness of 1 oz, the dielectric between then is of 10 mils. The dielectric substrate has a dielectric constant εr=4.6 (FR4), and a material dissipation factor tan (δ)=0.02. Also FR4 it has an intrinsic Rise Time of 30psec/in, which by using the following formula it gives with how much the rise time of a signal will increase depending on the length of the trace:

$$RT_{TL}=0.27 \times \tan\,(\delta) \times \sqrt{\varepsilon_r} \times d \text{ .... (9)}$$

Where RT_{TL} – represents the amount with which the rise time of the signal will increase, intrinsic rise time of the transmission line in ns, where:
εr: the complex dielectric constant.
d : the length of the transmission line, in inches.
tan(*δ*) : the material dissipation factor.

The S-parameters of the transmission line is plotted using the S-Parameter Simulation controller as shown in Figure (6). Figure (7) represents the insertion loss (S21) on printed circuit boards has become ever more critical to SI modeling as signal speeds required for next generation networking equipment move into 10GHz rang. From figure below, the transfer function (S21) is monotonically decreasing with increasing channel losses at higher frequencies.

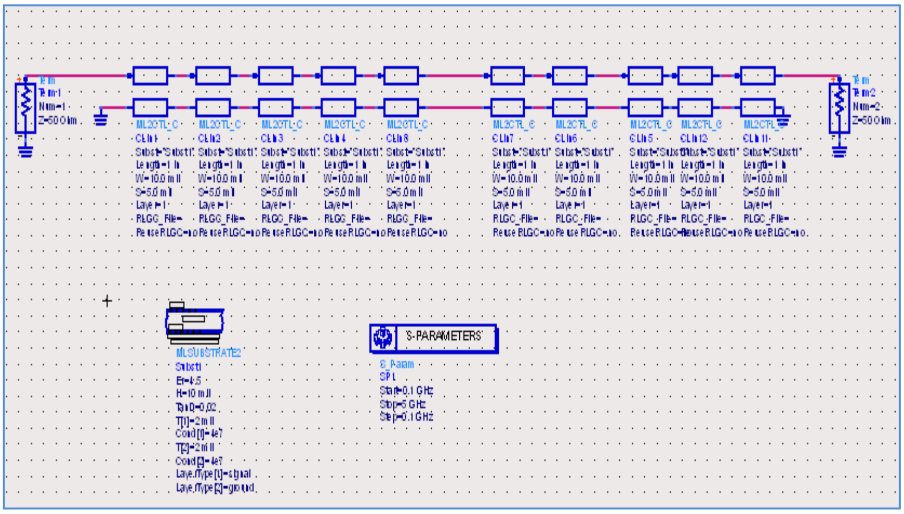


Fig. 6. S-parameter calculation of the channel

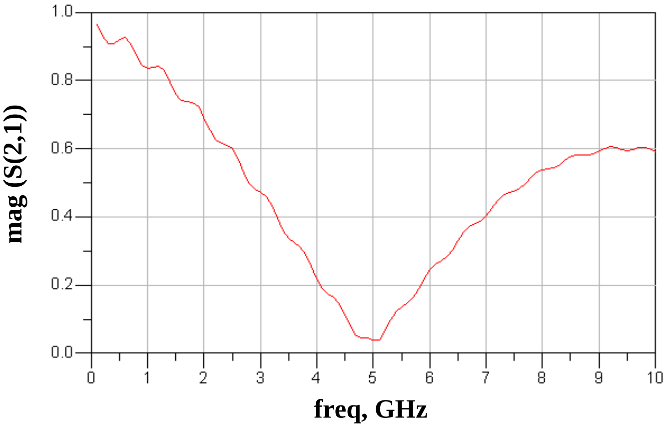


Fig. 7. Transmission line insertion loss plot

The system shown in Figure (5), represent A pseudo- random bit sequence (PRBS) (TX) is generated at a bit rate of 5 Gbps with number of bit=10000and bit by bit analysis mode where the maximum impulse response length (bit)=100 and number of time points per unit interval= 16, the voltage levels are V_{high}=1V, V_{Low}=0V and rise/ fall times is set as 30psec with equalization mode specifying FIR filter tap and tap interval equal 0.5 unit interval. The tap of the equlizer (FIR) filter in the TX is optimized using optimization properties of the simulator varying the tap coefficient to obtain optimum pre-emphasis level equal to 8.5dB and eliminate bit error. After adjusting the Tx side parameter we design the Rx component models a receiver. It includes equalization capabilities and random jitter injection. It also offers several options for modeling the receiver load. Up to one receiver component may be included in a simulation.

Adjust the parameter of the receiver side using channel simulator properties setting the electrical characteristic and enabling the equalization mode, and then we set the parameter of the Decision-Feedback Equalizer (DFE) as: slicer output equal 1/-1 with optimized weight tap according to the eye diagram shape which indicates the signal integrity. Depending on the eye diagram height we overrule the behavior of the designed system. The block diagram of the DFE circuit is shown in Figure (8) [9&10].

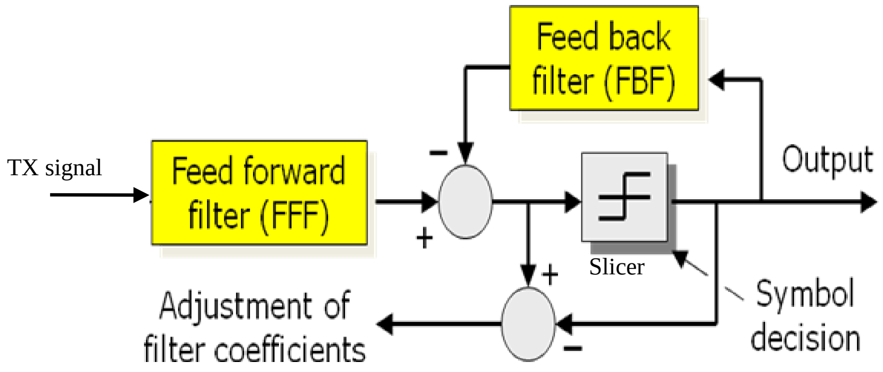
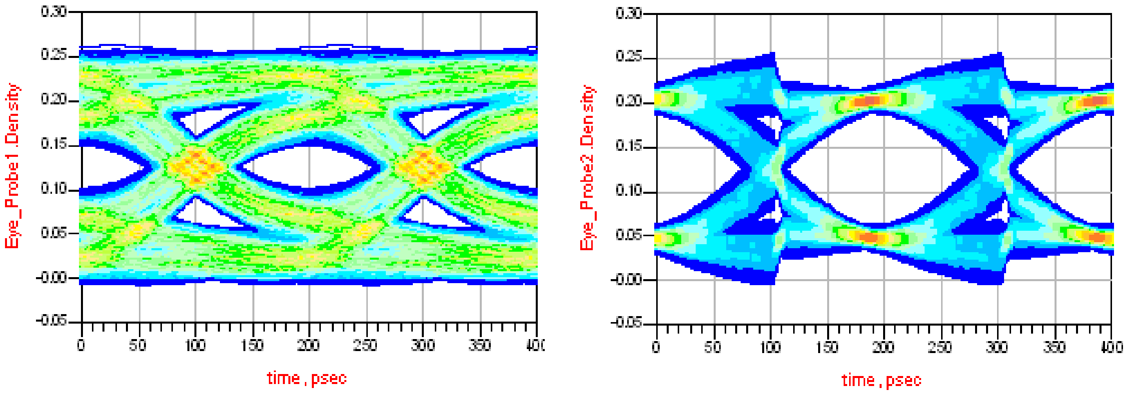


Fig. 8. Decision- Feedback Equalizer (DFE) circuit

However, the forward filter and the feedback filter can each be a linear filter, such as transversal filter. The nonlinearity of the DFE stems from the nonlinear characteristic of the detector that provides an input to the feedback filter. The basic idea of a DFE is that if the values of the symbols previously detected are known, then ISI contributed by these symbols can be canceled out exactly at the output of the forward filter by subtracting past symbol values with appropriate weighting. The forward and feedback tap can be adjusted simultaneously to minimize the MSE. The advantage of a DFE implementation is the feedback filter, which is additionally working to remove ISI, operates on noiseless quantized levels, and thus its output is free of channel noise.

The first case consider the under driven transmission line system under the data rate of 5Gb/s. the source resistance is chosen Rs=120Ω while the microstrip line has 50Ω characteristic impedance and 1in length. When Rs is larger than the characteristic impedance of the line it found that the reflected noises cause distortion in the edge transition thus the multiple reflections have significant impact on the signal equality. The output voltage in term of the eye diagram without any addition to the system and with the proposed circuit added is shown in Figure (9).

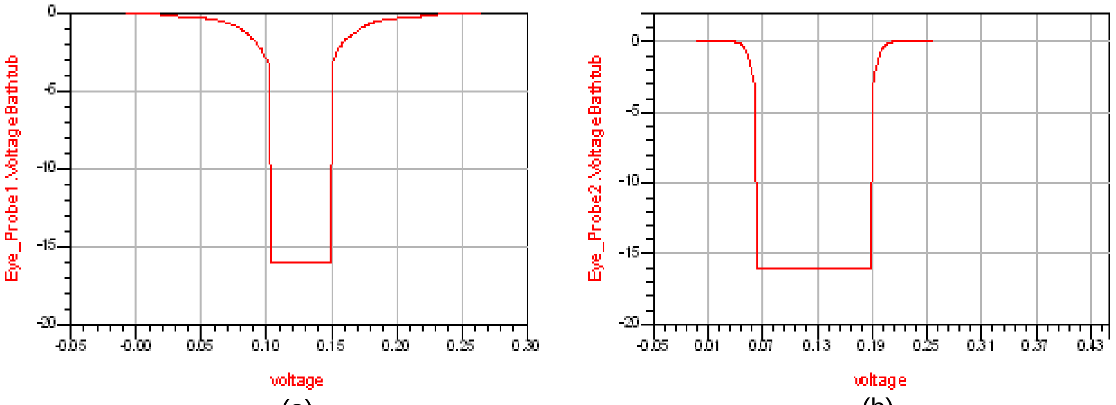


(a) (b)

Fig. 9. Simulated eye diagrams for the under driven line (a) before adding DFE and (b) with DFE in the RX circuit

From Figure (9a) we notice that the eye diagram is greatly deteriorated with eye height and eye width being 60mV and 111ps, respectively. After adding DFE to the RX circuit and after optimization of tap weighted of the feedback filter of the circuit we found that the 7tap is more suitable to improve the equality of the signal transmitted with total stopwatch time = 8.92 seconds. As a result, the eye diagram shown in Figure (9b) improves substantially with eye height and width being 1240mV and 170ps, or showing 196% and 53% improvement, respectively.

Figure (10) displaies voltage bathubs at the eye crossing level and eye center, respectively which represent the smallest voltage and timing margins give the bathtub curves as functions of voltage and time. It seen that the bathtub voltage in Figure (10b) is wider that in Figure (10a) that means The sampling voltage is scanned and the BER at each sampling point is recorded, so signal integrity is improve.

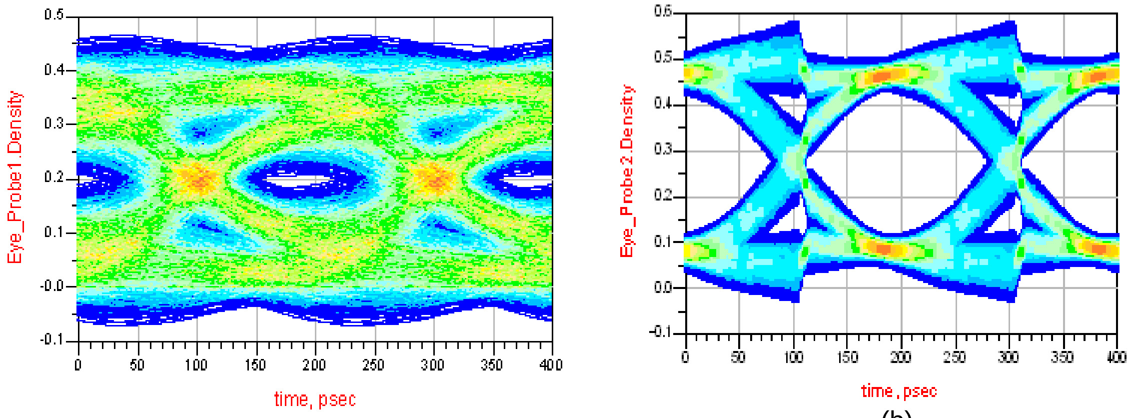


(a) (b)

Fig. 10. Bathtub voltage for the under driven line (a) before adding DFE and (b) with DFE in the RX circuit

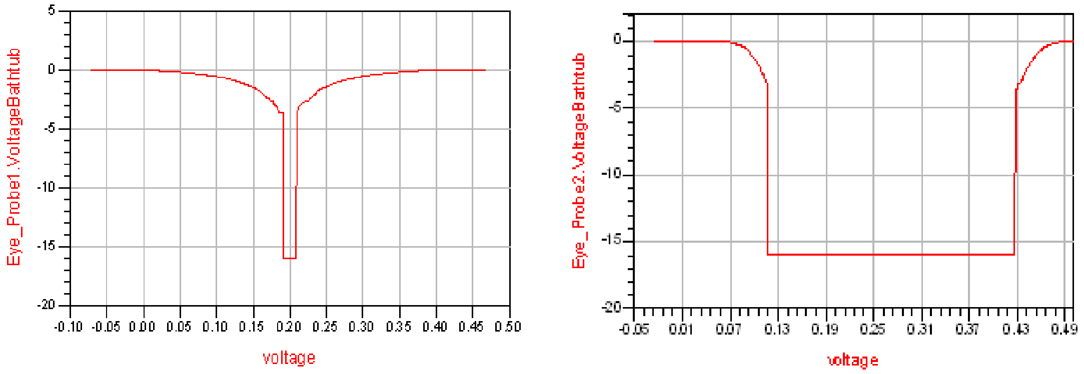
Another case commonly encountered in real applications is the overdriven transmission line where the source resistance is smaller than the characteristic impedance. For example, it is assumed that Rs=18Ω while all other parameters are the same as the precious case. The eye diagram waveform shown in Figure (11a) almost looks like closure with eye height and width being 90mV and 73ps, respectively.

For the overdriven line case according to the eye diagram the tap weight is optimized to set as the best tap number= 9tap with total stopwatch time equal to 10.94 second. As a result, the eye diagram shown in Figure (11b) improves substantially with eye height and width being 3090mV and 174ps, or showing 333% and 138% improvement, respectively. Figure (12) displaies voltage bathubs curves for sampling voltage.



(a) (b)

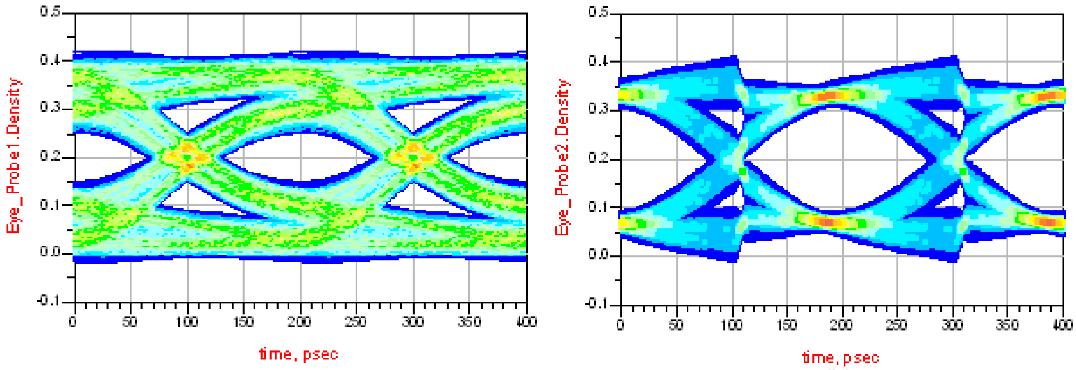
Fig. 11. Simulated eye diagrams for the overdriven line (a) before adding DFE and (b) with DFE in the RX circuit



(a) (b)

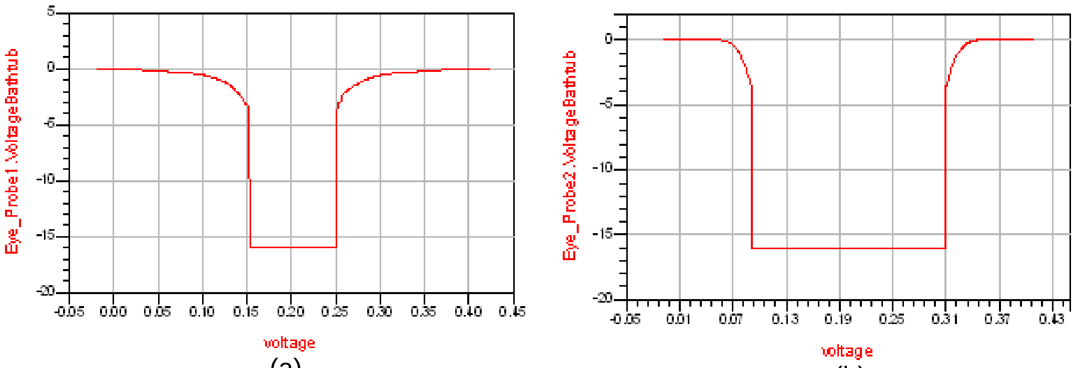
Fig. 12. Bathtub voltage curve for overdriven transmission line (a) before adding DFE and (b) with DFE in the RX circuit

The last case is for line length of 30in with matched termination (RS=RL=50Ω),with the same setting above eye diagram wave for before optimization of feedback filter tap in DFE in RX side is shown in Figure (13). It obvious from Figure (13a) that the frequency losses cause ISI problem which degrades the eye height and width to 89mVand 137ps, respectively. After adding the DFE circuit with optimized tap equal to 8 tap and total stop watch time equal to 9.09 seconds the resultant eye diagram have been increased to 215mV and 174ps or show 141% and 27% improvement, respectively, as compared with original case. Figure (14) Shows the bathtub voltage for lossy transmission line.



(a) (b)

Fig. 13. Simulated eye diagrams for the lossy line (a) before adding DFE and (b) with DFE in the RX circuit



(a) (b)

Fig. 14. Bathtub voltage curve for the lossy line (a) before adding DFE and (b) with DFE in the RX circuit

Conclusions

Decision Feedback Equalization (DFE) is one of the effective techniques to recover the signal at the receiver side from the signal distortion by ISI. The eye diagram observed at the receiver input node is no longer enough for the packaging system performance evaluation. In some applications, we also have to simulate and observe the eye diagram after DFE. In this paper an optimized DFE circuit is added to the receiver of transmission line system with high data rate and it obvious from the results that the designed circuit success to solve the problem of transmission line that affect the data transmitted on it the standard of it the opening improvement of the eye diagram present the data compared with the traditional methods and result obtained in [4] which use FIR filter as a pre-emphasis circuit on the transmitter where on the own paper we use the DFE circuit in addition to the FIR filter on the transmitter. The design demonstrates remarkable efficiency in the mitigation of the ISI effects incurred by multiple reflections in the unterminated line and lossy effect in the long transmission line. It is found that the eye height is improved by 196 % and 333% for under-and overdriven transmission line, respectively, as well as 141% for the long lossy transmission line. Also, a bathtube voltage curve demonstrates the voltage sampling period and the BER improvement of the tested transmission line system.

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